



H77H2-M3

Rev : A

ECS
CONFIDENTIAL

TABLE OF CONTENTS

Page	Index
1	COVER PAGE
2	Block Diagram
3	GPIO Function Map
4	CPU DMI/FDI/PEG
5	CPU MISC
6	CPU DDR3
7	CPU PWR
8	CPU GND
9	DDR3 CH_A_DIMM1
10	DDR3 CH_A_DIMM2
11	VCore & VAXG / RT8859M
12	VCore & VAXG / RT9612
13	DC/DC PCH / DRAM
14	DC/DC CPUVTT / RT8121
15	PCH DMI/PCI/PE/USB
16	PCH SATA
17	PCH MISC / Strap
18	PCH CLK IO / Clock GEN
19	PCH FDI / USB3.0


Page	Index
20	PCH DVI / HDMI / VGA
21	PCH PWR
22	PCH GND
23	Slot PCI-EX16 / PCI-EX1
24	DVI / HDMI
25	USB2/3.0 Conn & Header
26	SIO / ITE8728F-CX
27	PCIE LAN / RTL8111E
28	PCIE TO PCI / IT8893
29	Slot PCI1 / 2
30	AUDIO CODEC / ALC662
31	AUDIO PANEL
32	F_Panel / FAN / PWR CONN
33	LPT / COM / PS2
34	TPM / 104
35	Power Delivery
36	Power Sequence, Reset Diagram
37	Clock Distribution

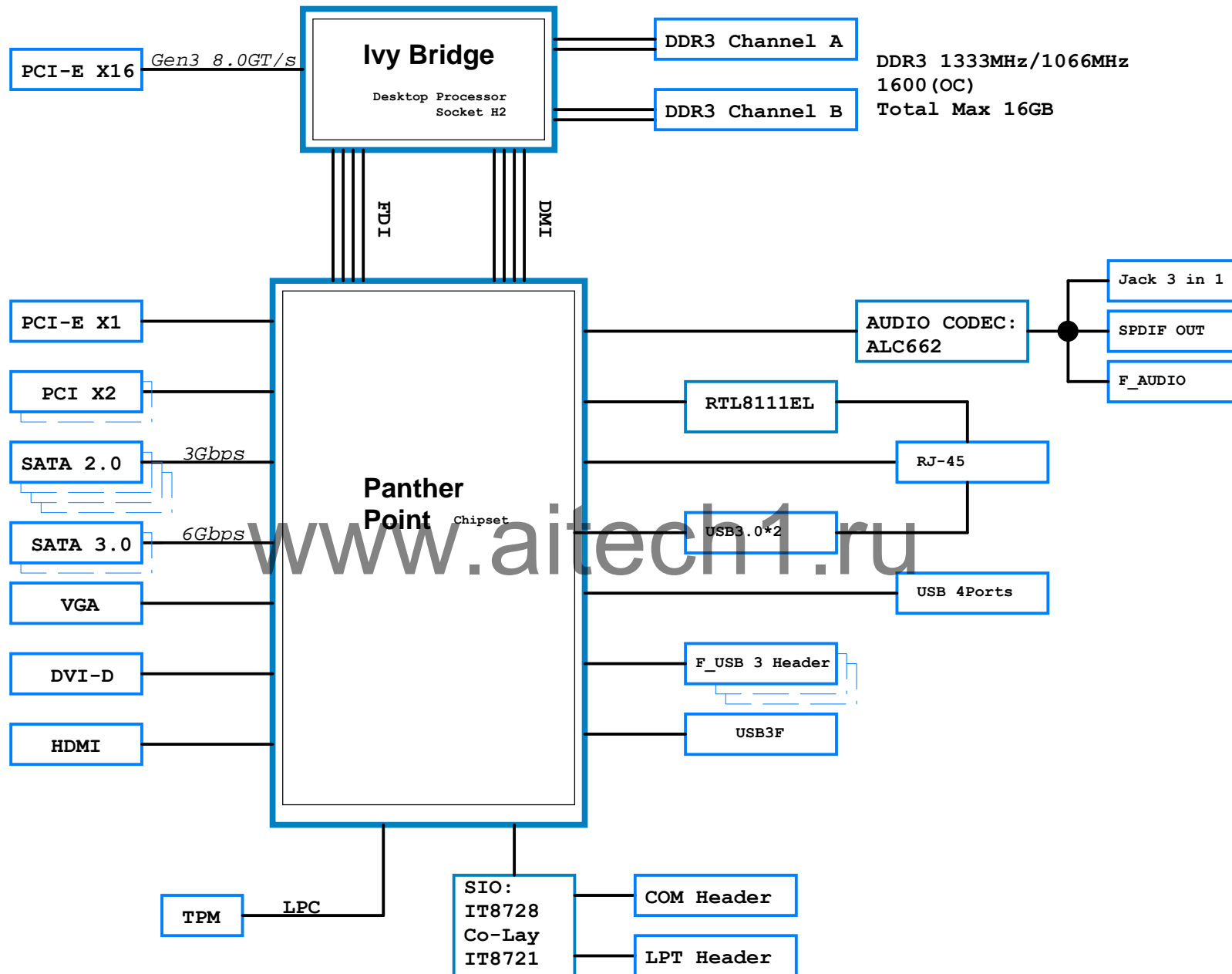
REVISION HISTORY:

Rev	Date	Notes
V A(H61H2-M7)	2011/06/21	Initial version

NOTE:

1. Model Code: ED7
2. Modified from H61H2-M7 V 1.0

 Elitegroup Computer Systems		
Title Cover Page		
Size Custom	Document Number H77H2-M3	Rev A
Date: Monday, July 18, 2011	Sheet 1	of 37



PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3	VT1705CD/VT1705CE	GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI

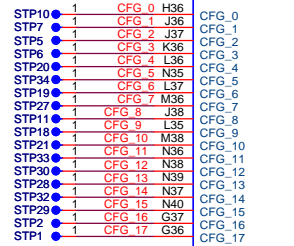
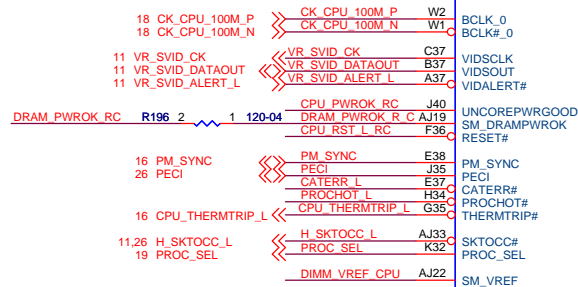
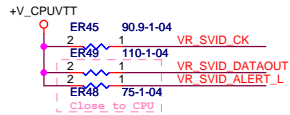
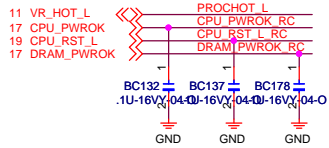
SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16		BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	

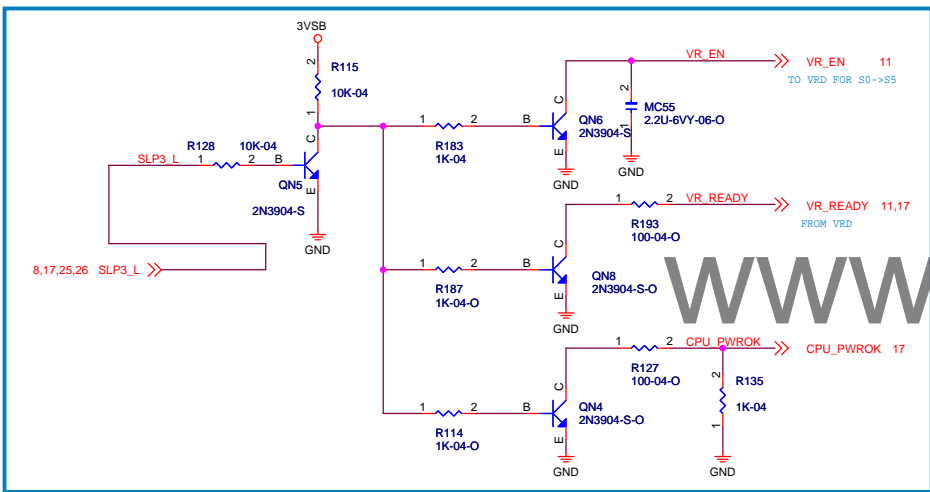
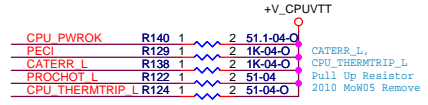
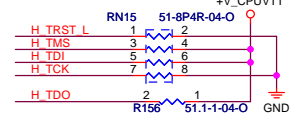
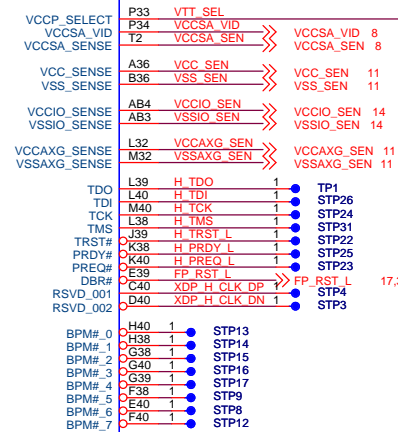
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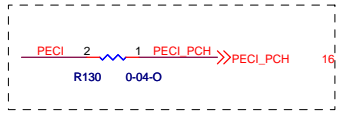
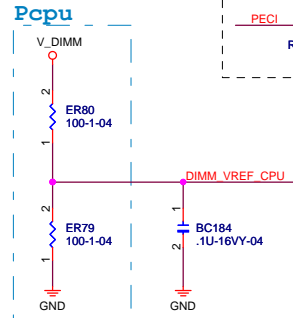
DMI/FDI TERMINATION VOLTAGE
 DC COUPLED: TX/RX TO VCC IF SAMPLED HIGH
 DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
 AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



BALLMAP_REV=1.4



Power Down Sequencing Circuit



CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG [0..17] HAVE INTERNAL PULL-UPS

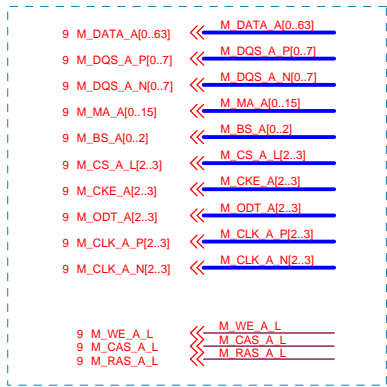
PCIE CONFIG	SELO	SEL1
1 X 16	1	1
2 X 8	0	1

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Title: **CPU MISC**

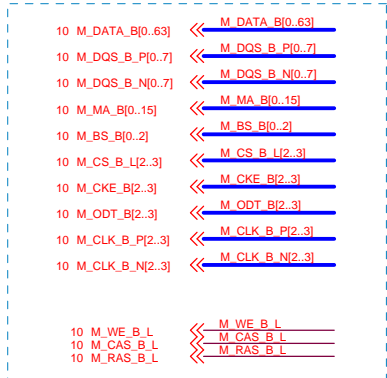
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Date: Monday, July 18, 2011 Sheet: 5 of 37

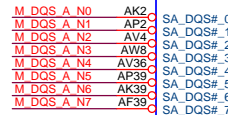
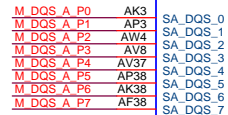
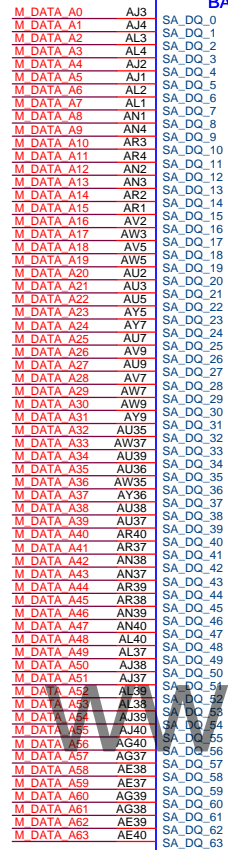


DDR3 CH.A

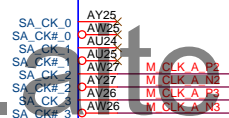
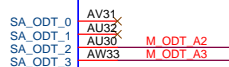
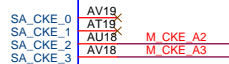
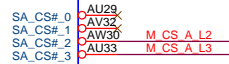
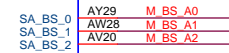
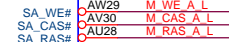
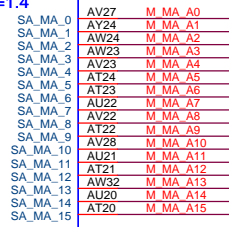
9,10 DDR3_DRAMRST_L <-> DDR3_DRAMRST_L



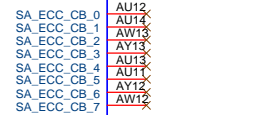
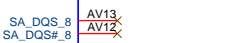
DDR3 CH.B



BALLMAP_REV=1.4



SM_DRAMRST# AW18 DDR3_DRAMRST_L



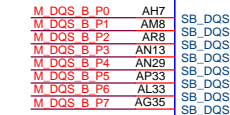
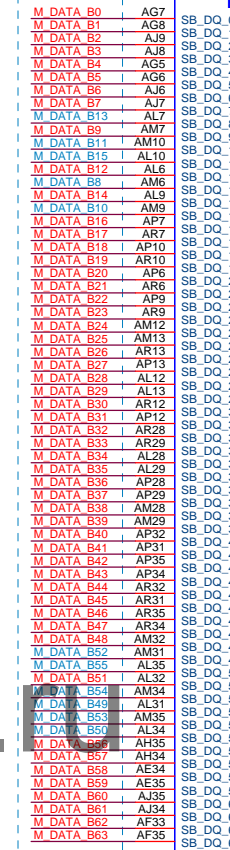
DDR_0

3 OF 10

LGA-1155P-S

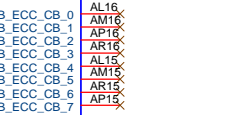
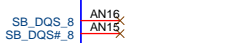
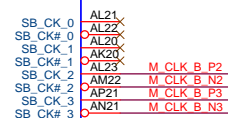
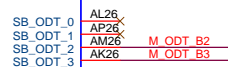
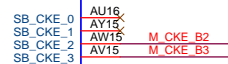
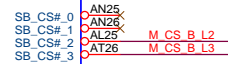
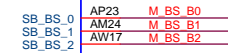
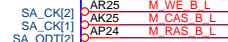
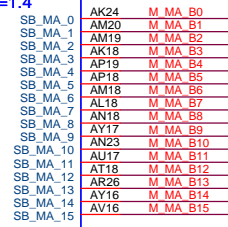
DDR3 CH.A

Pay Attention to This Part!



CPUD

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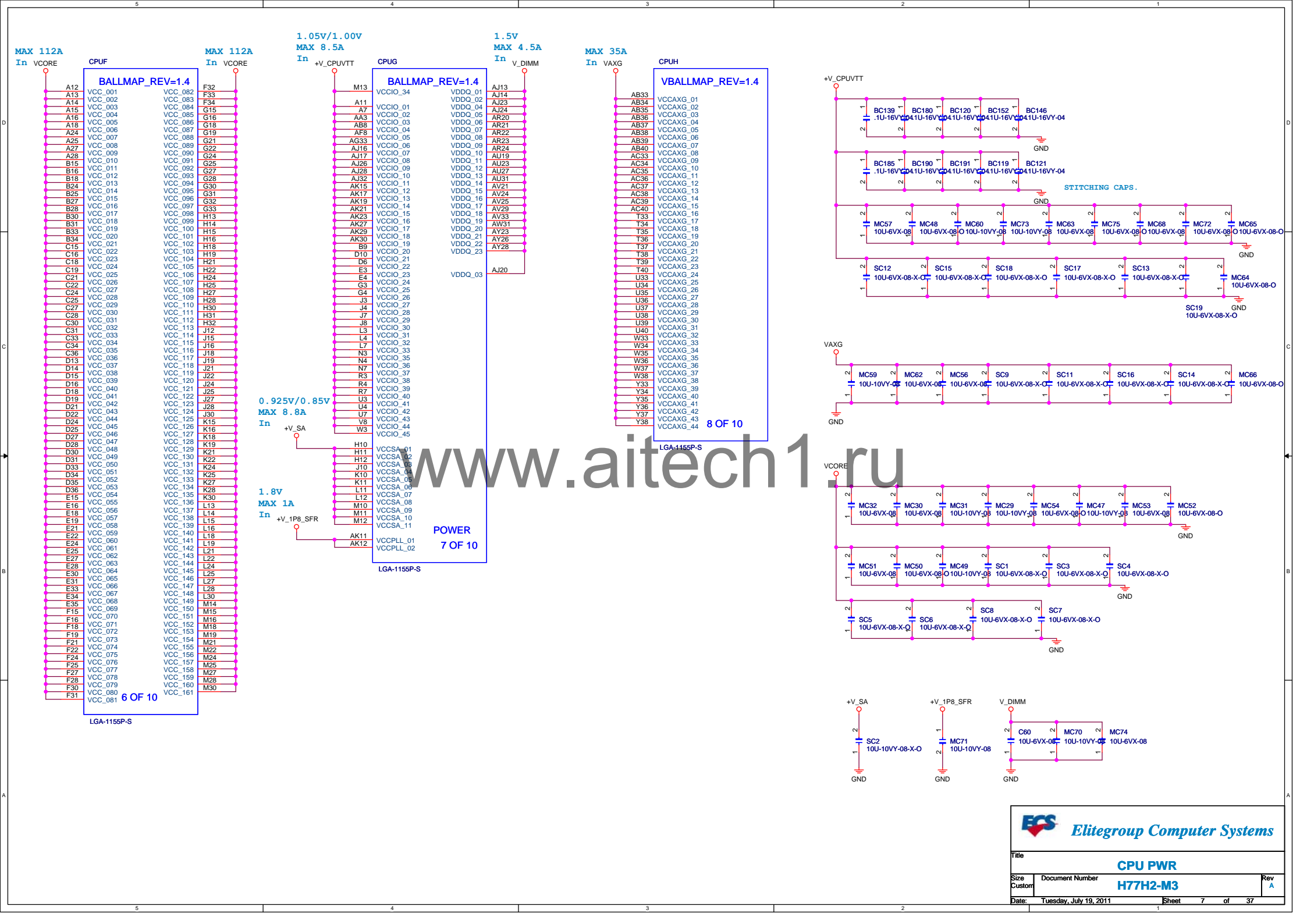


DDR_1

4 OF 10

LGA-1155P-S

DDR3 CH.B



CPU1

BALLMAP_REV=1.4

A17	VSS_001	AM27
A23	VSS_002	AM3
A26	VSS_003	AM30
A29	VSS_004	AM36
AA35	VSS_005	AM37
AA33	VSS_006	AM38
AA34	VSS_007	AM39
AA35	VSS_008	AM4
AA36	VSS_009	AM40
AA37	VSS_010	AM5
AA38	VSS_011	AN10
AA6	VSS_012	AN11
AB5	VSS_013	AN12
AC1	VSS_014	AN17
AC6	VSS_015	AN19
AD33	VSS_016	AN22
AD36	VSS_017	AN24
AD38	VSS_018	AN27
AD39	VSS_019	AN30
AD40	VSS_020	AN31
AD5	VSS_021	AN32
AD8	VSS_022	AN33
AE3	VSS_023	AN34
AE33	VSS_024	AN35
AE36	VSS_025	AN36
AF1	VSS_026	AN5
AF34	VSS_027	AN6
AF36	VSS_028	AN8
AF37	VSS_029	AN9
AF40	VSS_030	AP1
AF6	VSS_032	AP11
AF7	VSS_033	AP14
AG36	VSS_034	AP17
AH2	VSS_035	AP22
AH3	VSS_036	AP25
AH33	VSS_037	AP27
AH36	VSS_038	AP30
AH37	VSS_039	AP36
AH38	VSS_040	AP37
AH39	VSS_041	AP4
AH40	VSS_042	AP40
AH5	VSS_043	AP5
AH8	VSS_044	AR11
AJ12	VSS_045	AR14
AJ15	VSS_046	AR17
AJ18	VSS_047	AR18
AJ21	VSS_048	AR19
AJ25	VSS_049	AR27
AJ27	VSS_050	AR30
AJ36	VSS_051	AR36
AJ5	VSS_052	AR5
AK1	VSS_053	AT1
AK10	VSS_054	AT10
AK13	VSS_055	AT12
AK14	VSS_056	AT13
AK16	VSS_057	AT15
AK22	VSS_058	AT16
AK28	VSS_059	AT17
AK31	VSS_060	AT2
AK32	VSS_061	AT25
AK33	VSS_062	AT27
AK34	VSS_063	AT28
AK35	VSS_064	AT29
AK36	VSS_065	AT3
AK37	VSS_066	AT30
AK4	VSS_067	AT31
AK40	VSS_068	AT32
AK5	VSS_069	AT33
AK6	VSS_070	AT34
AK7	VSS_071	AT35
AK8	VSS_072	AT36
AK9	VSS_073	AT38
AL11	VSS_074	AT39
AL14	VSS_075	AT4
AL17	VSS_076	AT40
AL19	VSS_077	AT5
AL24	VSS_078	AT6
AL27	VSS_079	AT7
AL30	VSS_080	AT8
AL36	VSS_081	AT9
AL5	VSS_082	AU1
AM1	VSS_083	AU15
AM11	VSS_084	AU26
AM14	VSS_085	AU34
AM17	VSS_086	AU4
AM2	VSS_087	AU6
AM21	VSS_088	AU8
AM23	VSS_089	AU10
AM25	VSS_090	

A4 VSS_NCTF_01 9 OF 10

AV39 VSS_NCTF_02

LGA-1155P-S

CPU1

BALLMAP_REV=1.4

AV11	VSS_181	VSS_271
AV14	VSS_182	H1
AV17	VSS_183	H17
AV3	VSS_184	H2
AV35	VSS_185	H20
AV38	VSS_186	H23
AV6	VSS_187	H26
AW10	VSS_188	H29
AW11	VSS_189	H33
AW14	VSS_190	H37
AW16	VSS_191	H39
AW36	VSS_192	H5
AW6	VSS_193	H6
AY11	VSS_194	H9
AY14	VSS_195	J11
AY18	VSS_196	J17
AY35	VSS_197	J20
AY4	VSS_198	J23
AY6	VSS_199	J26
AY8	VSS_200	J29
B10	VSS_201	J32
B13	VSS_202	J37
B14	VSS_203	K12
B17	VSS_204	K13
B23	VSS_205	K14
B26	VSS_206	K17
B29	VSS_207	K2
B32	VSS_208	K20
B35	VSS_209	K23
B38	VSS_210	K26
B6	VSS_211	K29
C11	VSS_212	K33
C12	VSS_213	K35
C17	VSS_214	K37
C20	VSS_215	K39
C23	VSS_216	K5
C26	VSS_217	K6
C29	VSS_218	L10
C32	VSS_219	L17
C35	VSS_220	L20
C7	VSS_221	L23
C8	VSS_222	L26
D17	VSS_223	L29
D2	VSS_224	L8
D20	VSS_225	M1
D23	VSS_226	M17
D26	VSS_227	M2
D29	VSS_228	M20
D32	VSS_229	M23
D37	VSS_230	M26
D39	VSS_231	M29
D4	VSS_232	M33
D5	VSS_233	M35
D9	VSS_234	M37
E11	VSS_235	M39
E12	VSS_236	M5
E17	VSS_237	M6
E20	VSS_238	M9
E23	VSS_239	N8
E26	VSS_240	P1
E29	VSS_241	P2
E32	VSS_242	P36
E36	VSS_243	P38
E7	VSS_244	P40
E8	VSS_245	P5
F1	VSS_246	P6
F10	VSS_247	P33
F13	VSS_248	P35
F14	VSS_249	P37
F17	VSS_250	P39
F2	VSS_251	R8
F20	VSS_252	T1
F23	VSS_253	T5
F26	VSS_254	T6
F29	VSS_255	U8
F35	VSS_256	V1
F37	VSS_257	V2
F39	VSS_258	V33
F5	VSS_259	V34
F6	VSS_260	V35
F9	VSS_261	V36
G11	VSS_262	V37
G12	VSS_263	V38
G17	VSS_264	V39
G20	VSS_265	V40
G23	VSS_266	V5
G26	VSS_267	W6
G29	VSS_268	Y5
G34	VSS_269	Y8
G7	VSS_270	

AY37 VSS_NCTF_03 10 of 10

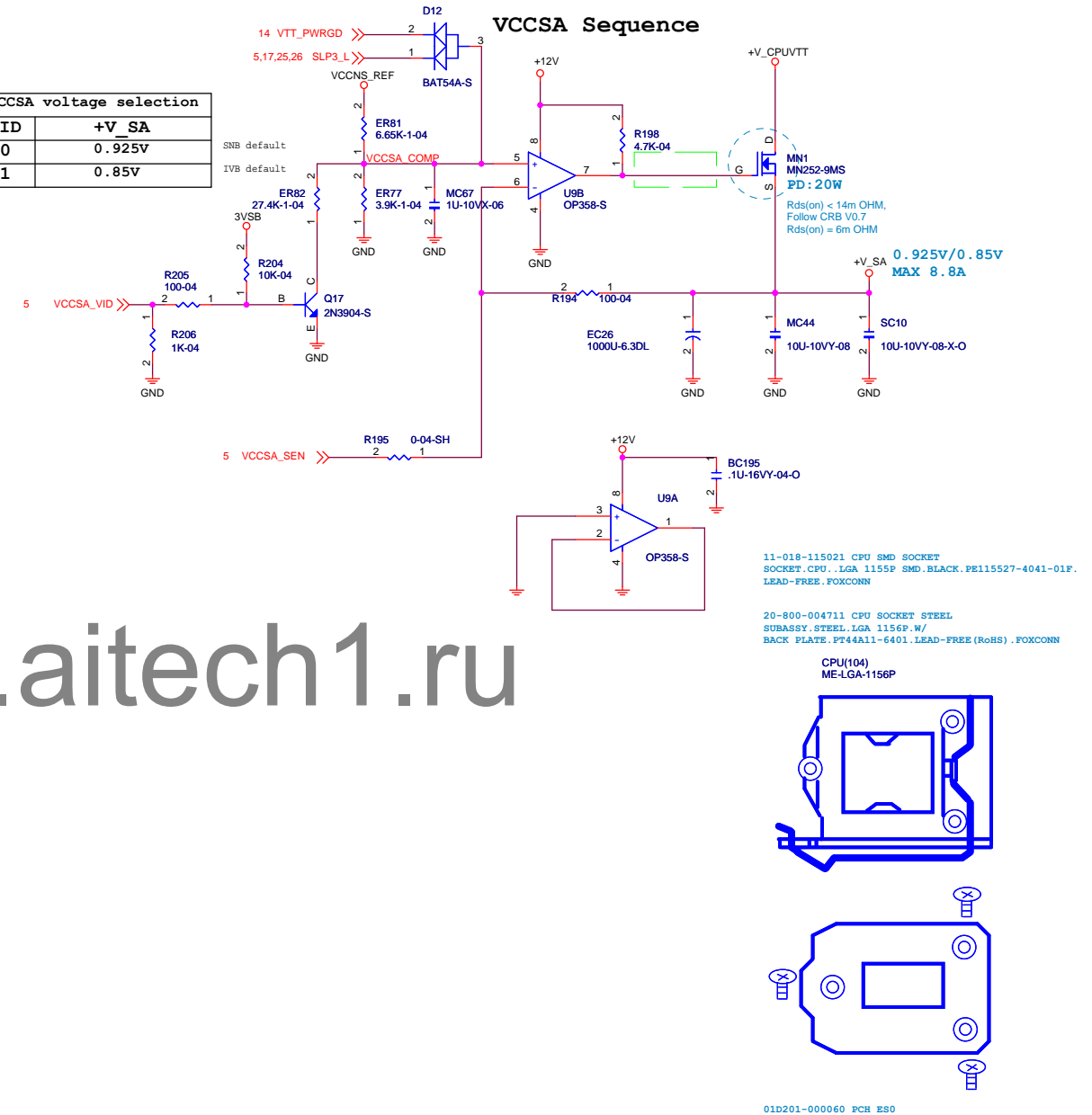
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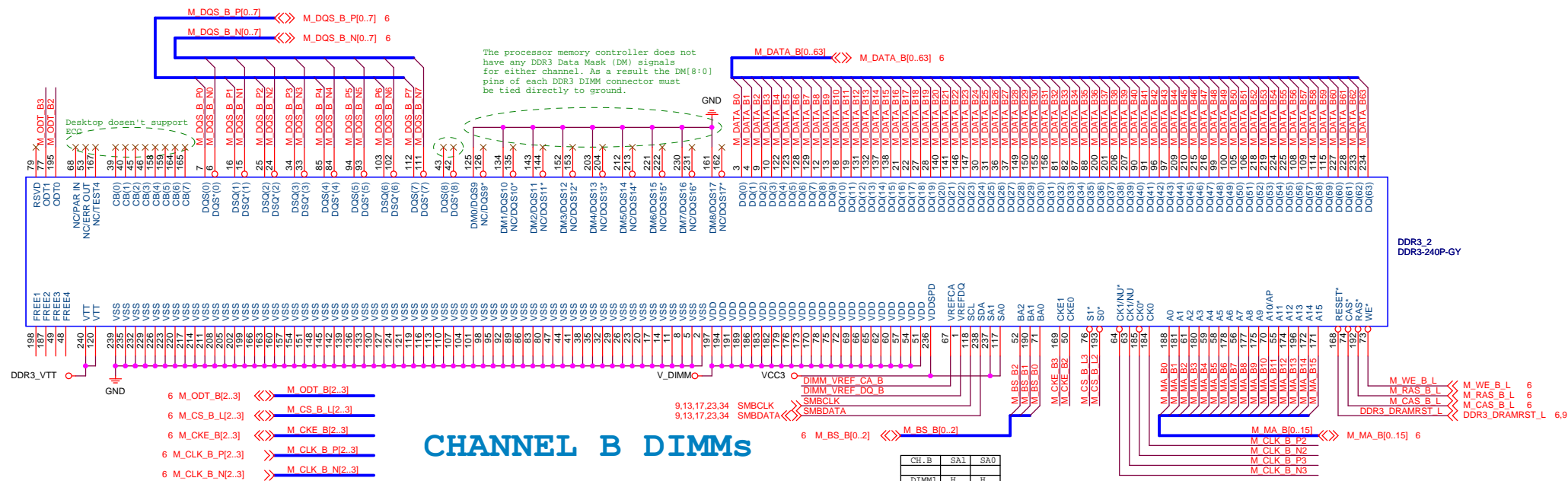
LGA-1155P-S

VCCSA voltage selection

VID	+V_SA
0	0.925V
1	0.85V

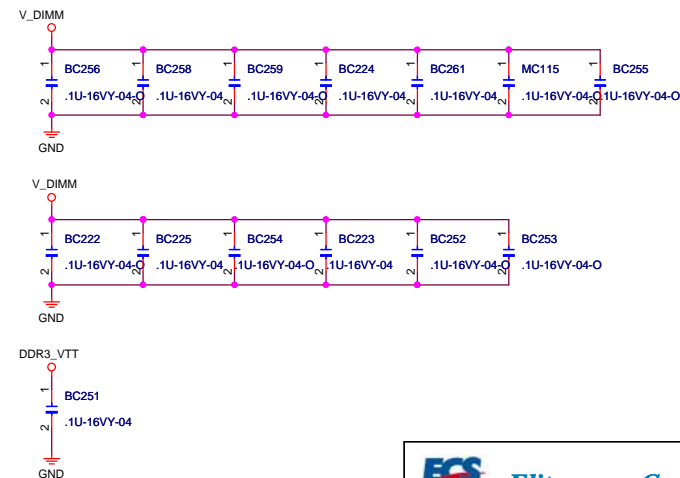
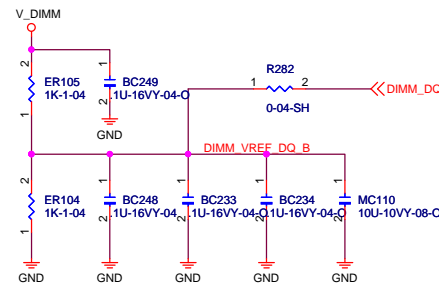
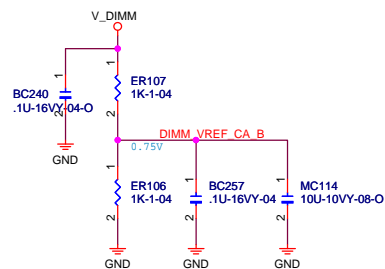
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CHANNEL B DIMMs

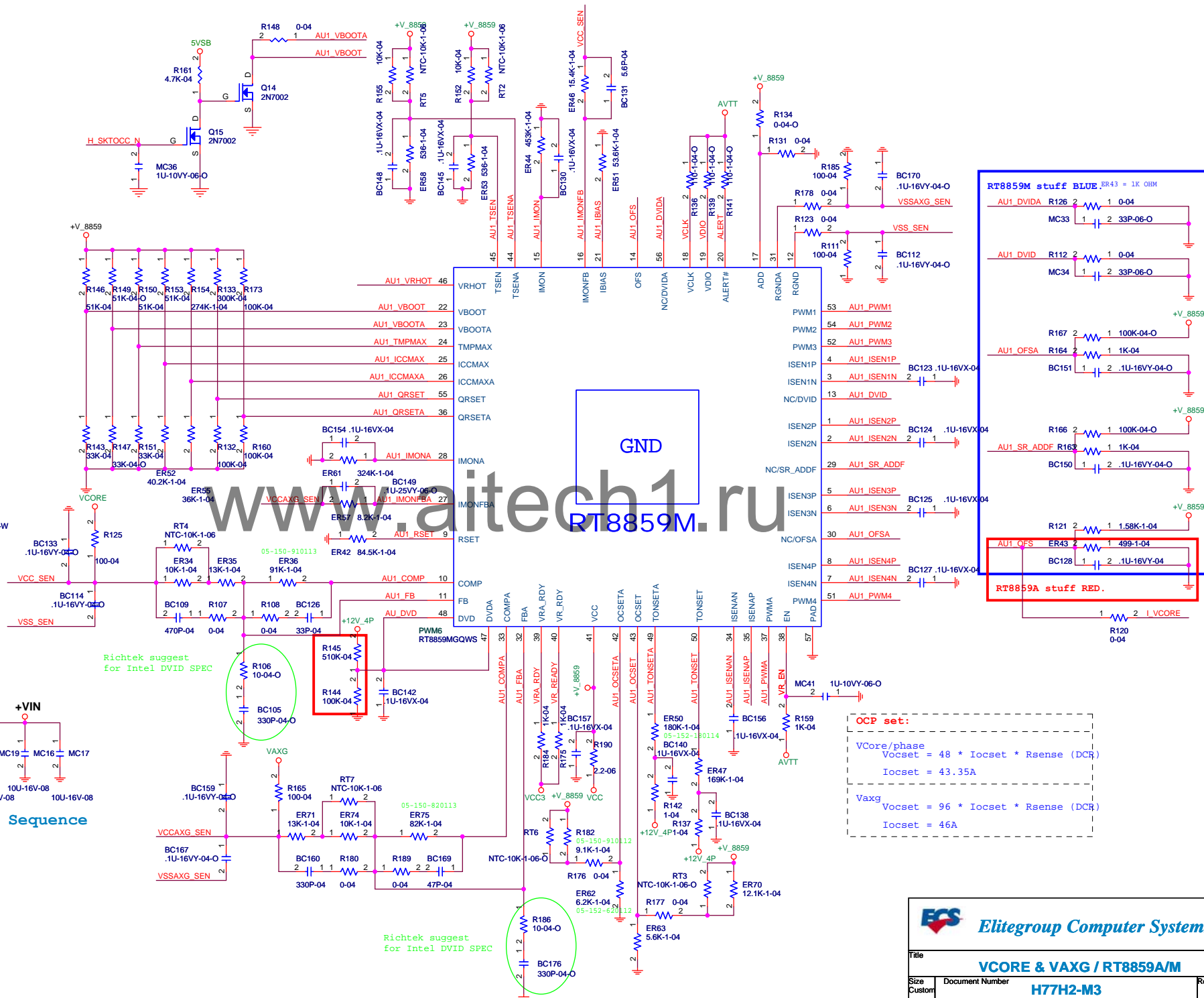
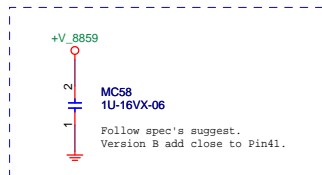
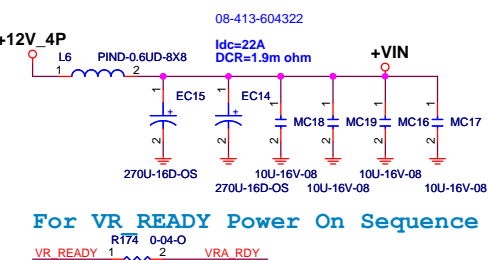
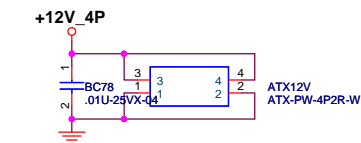
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External Connection

Pin connections for External Connection:

- VCC to VCC
- +V_CPUVTT to AVTT
- +12V_4P to +12V_4P
- VCC3 to OVCC3
- +VIN to +VIN
- 5VSB to 5VSB
- VR_EN to VR_EN
- VR_SVID_ALERT_L to ALERT
- VR_SVID_DATA_OUT_L to VDBIO
- VR_SVID_CLK to VCLK
- VR_HOT_L to AU1_VRHOT
- AU1_PWM[1..4] to AU1_PWM[1..4]
- AU1_ISEN1P to AU1_ISEN1P
- AU1_ISEN1N to AU1_ISEN1N
- AU1_ISEN2P to AU1_ISEN2P
- AU1_ISEN2N to AU1_ISEN2N
- AU1_ISEN3P to AU1_ISEN3N
- AU1_ISEN3N to AU1_ISEN3N
- AU1_ISEN4P to AU1_ISEN4P
- AU1_ISEN4N to AU1_ISEN4N
- VCC_SEN to VCC_SEN
- VSS_SEN to VSS_SEN
- VR_READY to VR_READY
- AU1_PWMMA to AU1_PWMMA
- AU1_ISENAP to AU1_ISENAP
- AU1_ISENAN to AU1_ISENAN
- VCCAXG_SEN to VCCAXG_SEN
- VSSAXG_SEN to VSSAXG_SEN
- I_VCORE to I_VCORE
- H_SKT0CC_L to H_SKT0CC_N



External Connection



11 AU1_PWM[1..4] AU1_PWM[1..4]

11 AU1_ISEN1P AU1_ISEN1P

11 AU1_ISEN1N AU1_ISEN1N

11 AU1_ISEN2P AU1_ISEN2P

11 AU1_ISEN2N AU1_ISEN2N

11 AU1_ISEN3P AU1_ISEN3P

11 AU1_ISEN3N AU1_ISEN3N

11 AU1_ISEN4P AU1_ISEN4P

11 AU1_ISEN4N AU1_ISEN4N

5,11 VCC_SEN VCC_SEN

5,11 VSS_SEN VSS_SEN

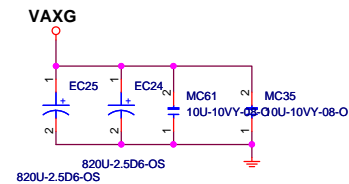
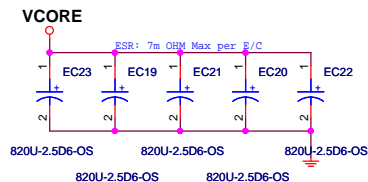
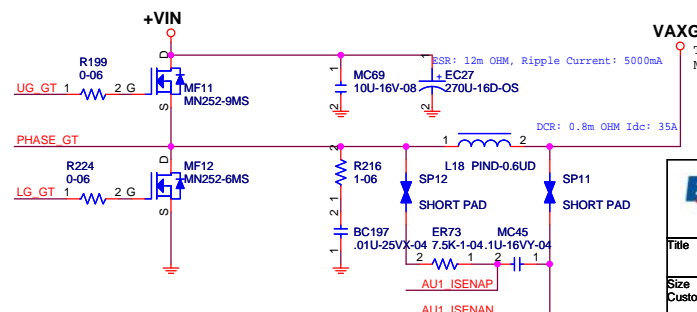
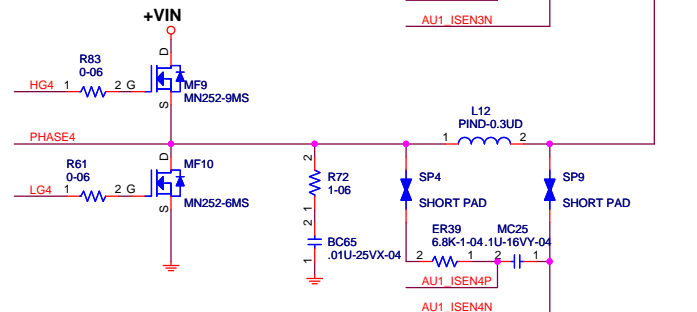
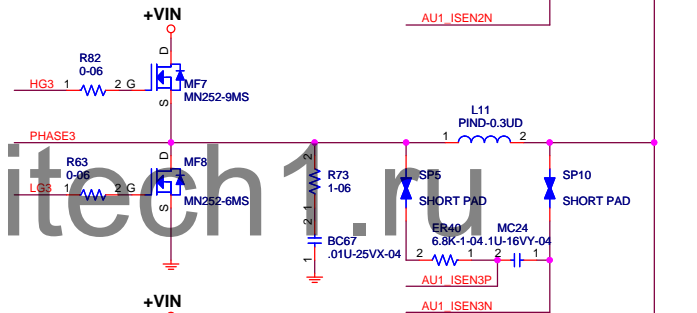
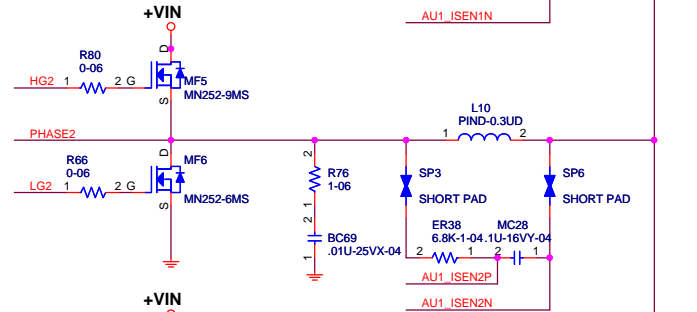
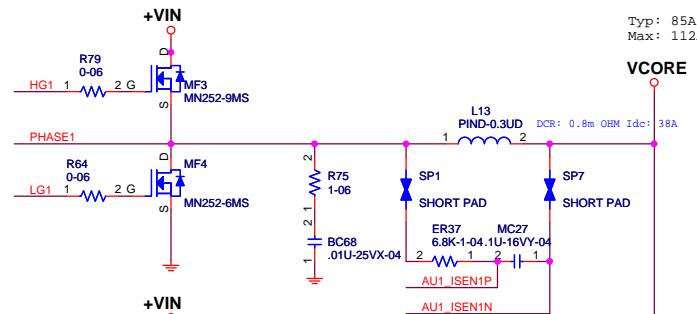
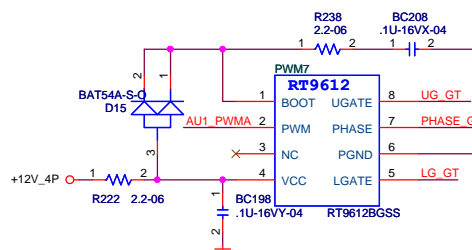
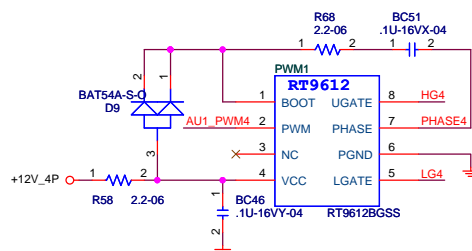
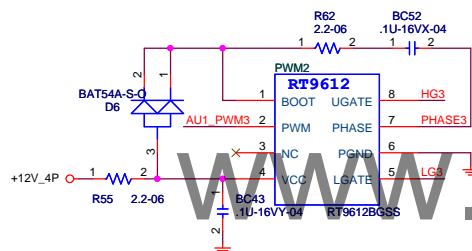
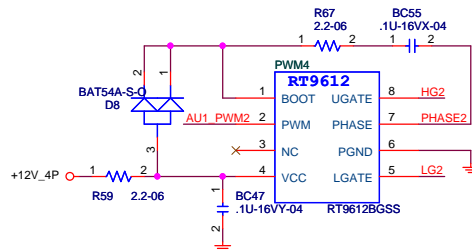
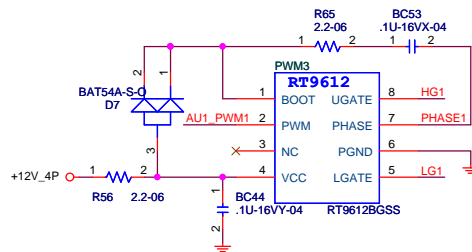
11 AU1_PWMA AU1_PWMA

11 AU1_ISENAP AU1_ISENAP

11 AU1_ISENAN AU1_ISENAN

5,11 VCCAXG_SEN VCCAXG_SEN

5,11 VSSAXG_SEN VSSAXG_SEN



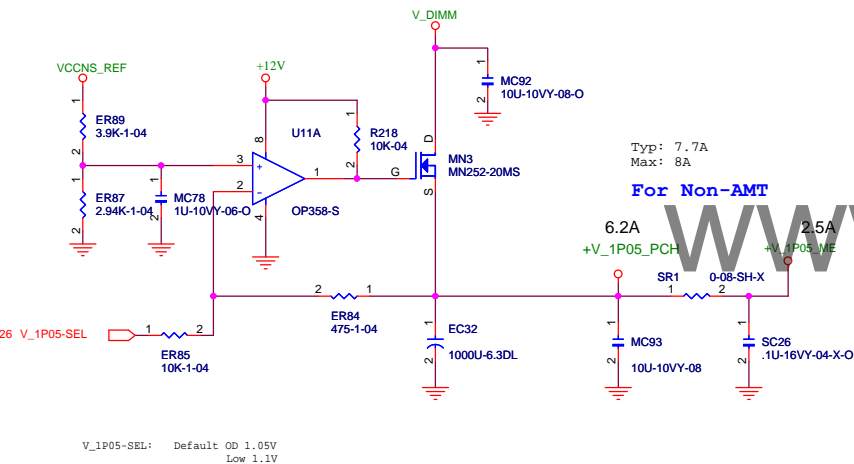
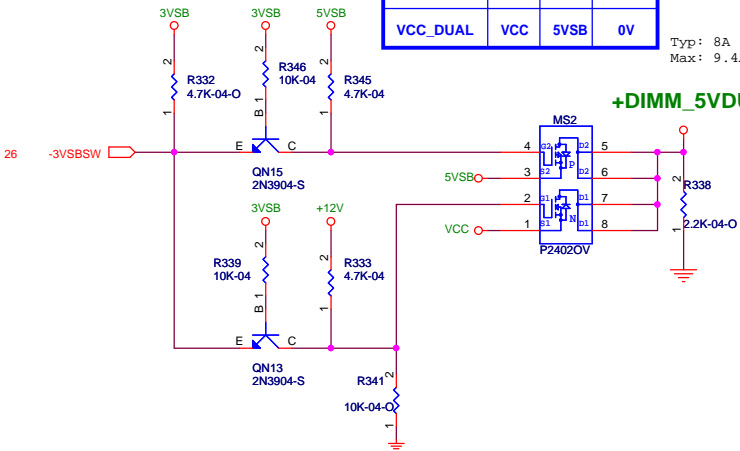
Elitegroup Computer Systems

Title	VCORE & VAXG / RT9612		
Size	Document Number	H77H2-M3	
Custom		Rev A	
Date:	Monday, July 18, 2011	Sheet	12 of 37

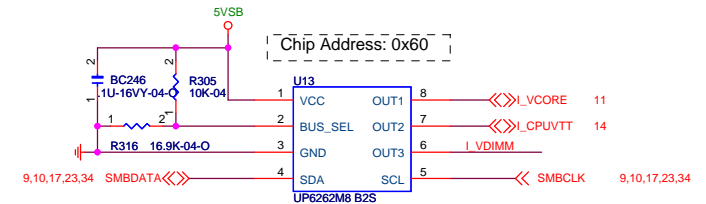
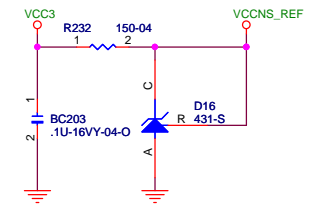
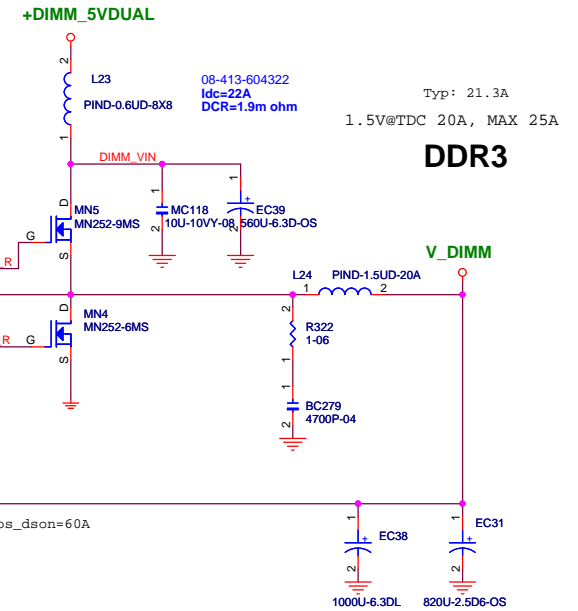
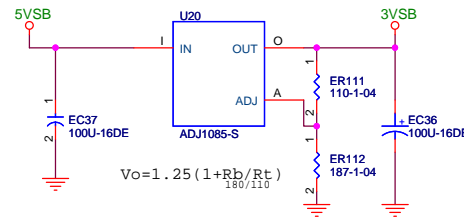
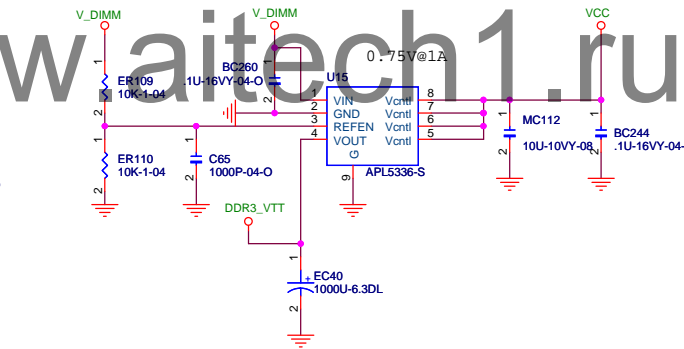
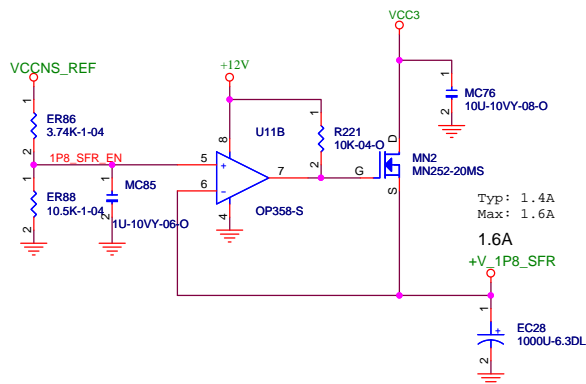
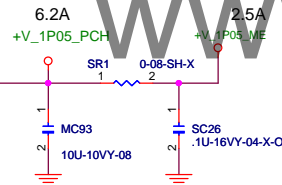
	S0	S3	S4/S5
S3_SW	H	L	H
VCC_DUAL	VCC	5VSB	0V

Typ: 8A
Max: 9.4A

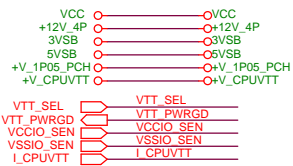
+DIMM_5VDUAL



For Non-AMT



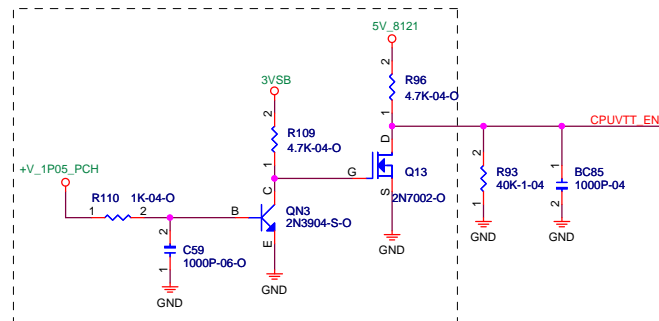
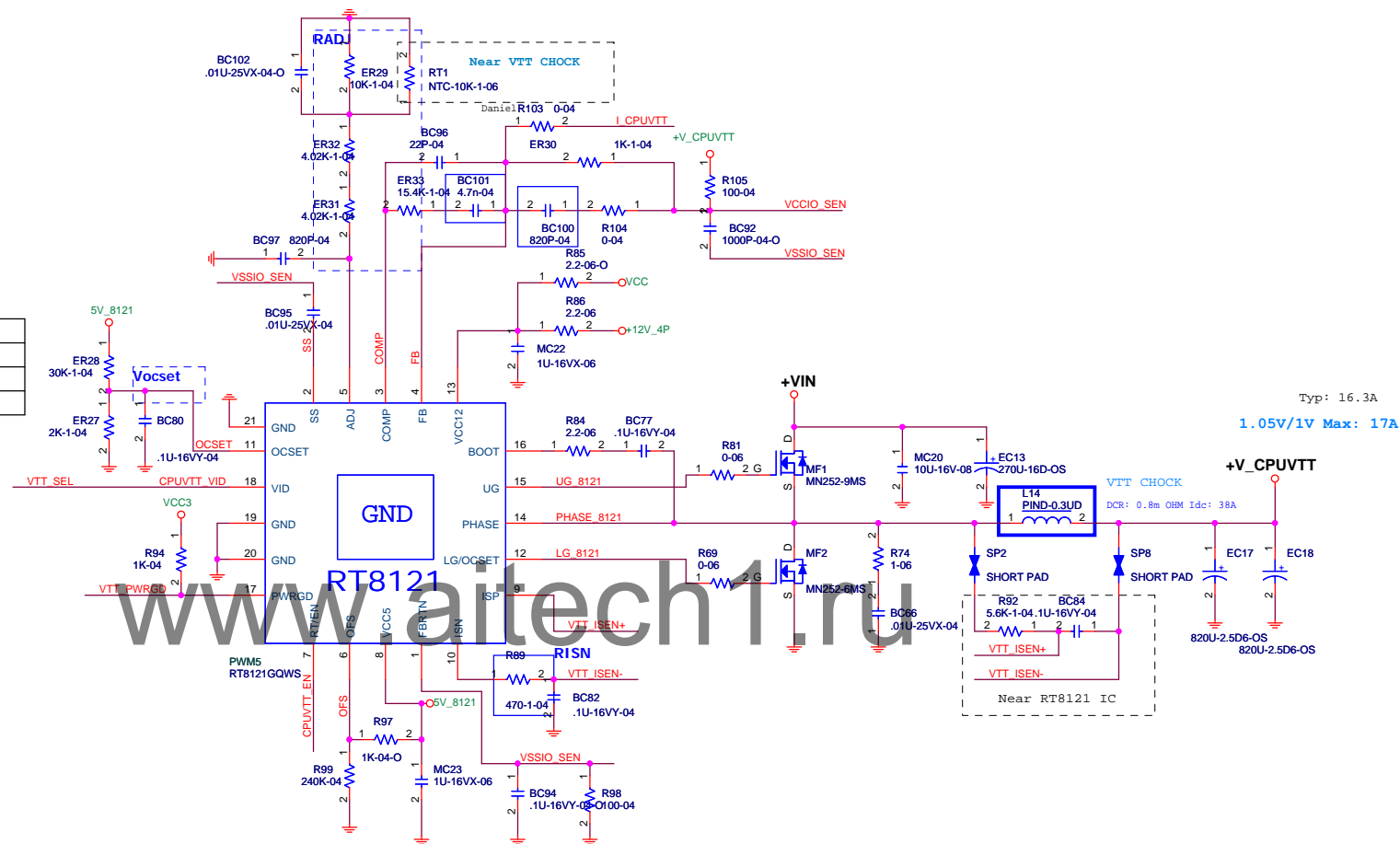
External Connection

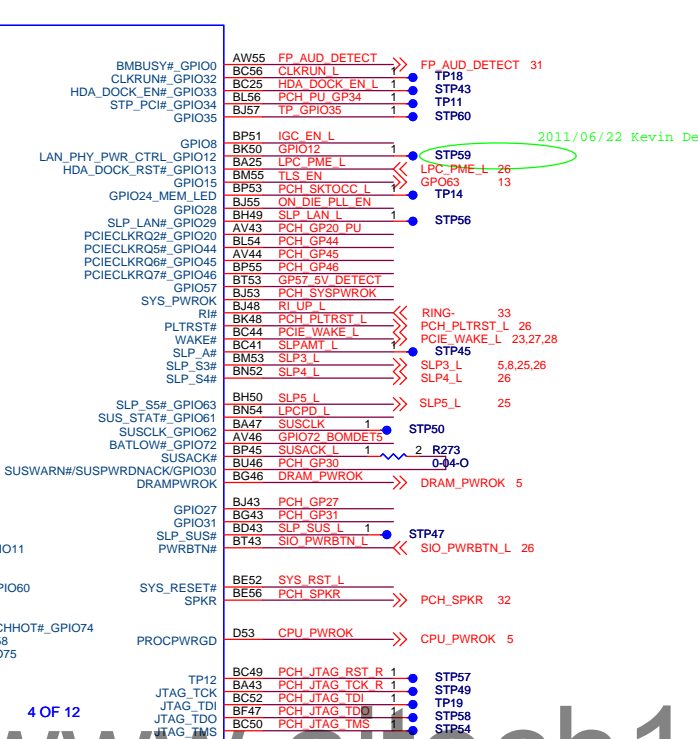
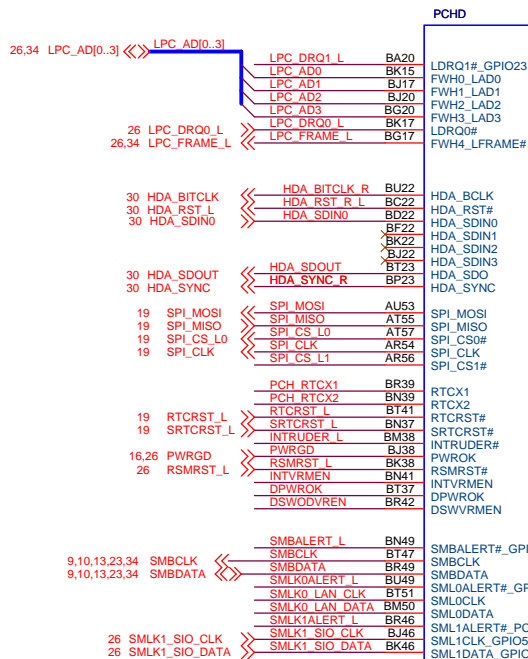


VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V

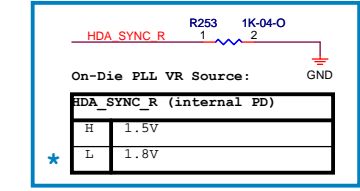
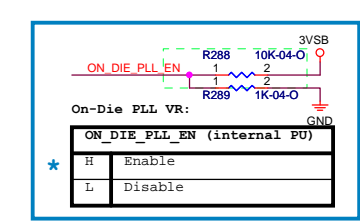
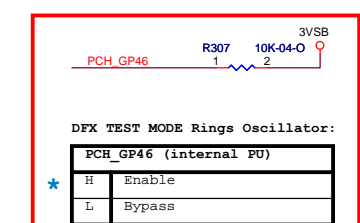
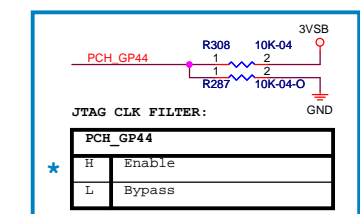
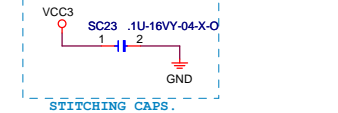
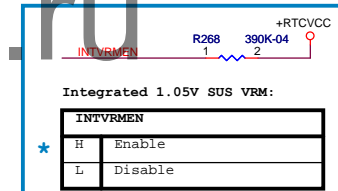
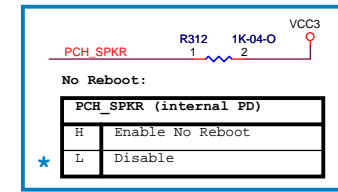
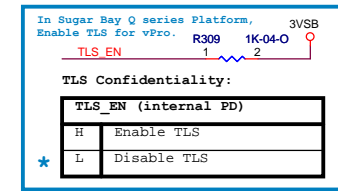
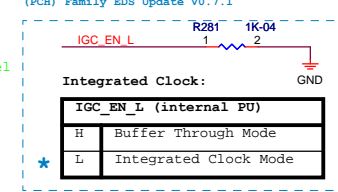
OCP set:

$$\begin{aligned} \text{Vocset} &= 1/2 * I_x * \text{RADJ} \\ &= 1/2 * (I_L * \text{DCR} / \text{RISN}) * \text{RADJ} \\ \text{Iocset} &= 31.7\text{A} \\ &= 1.82 * \text{Imax} \end{aligned}$$

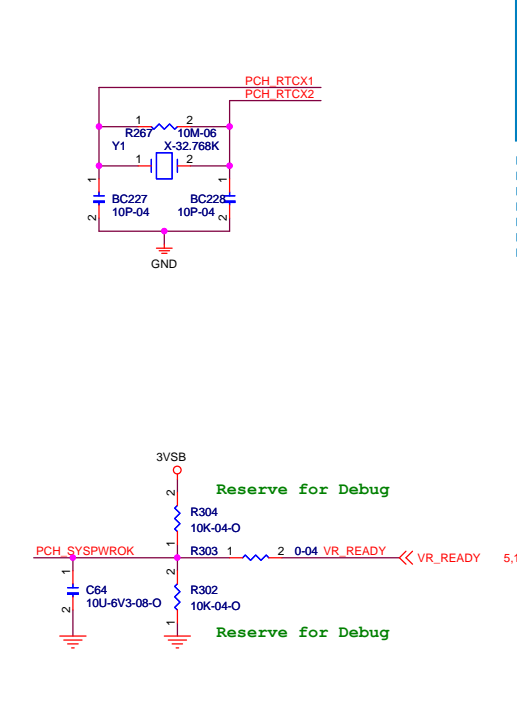
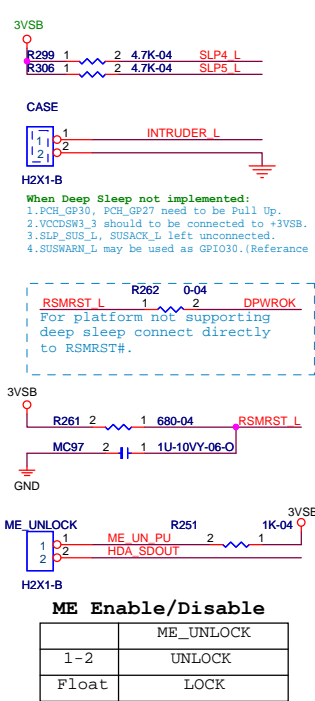
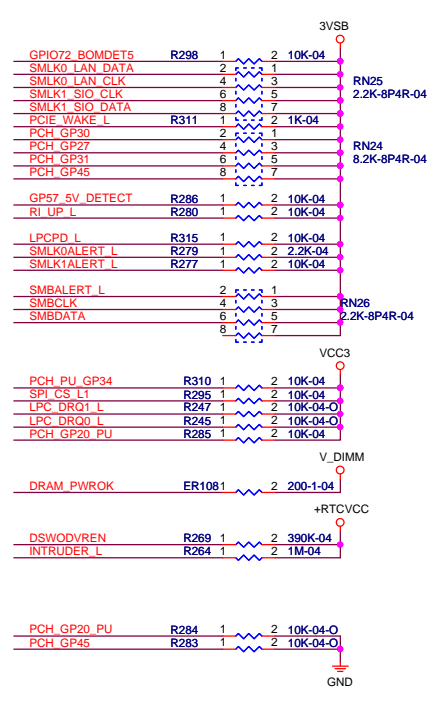
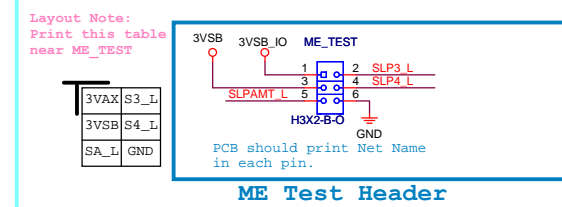


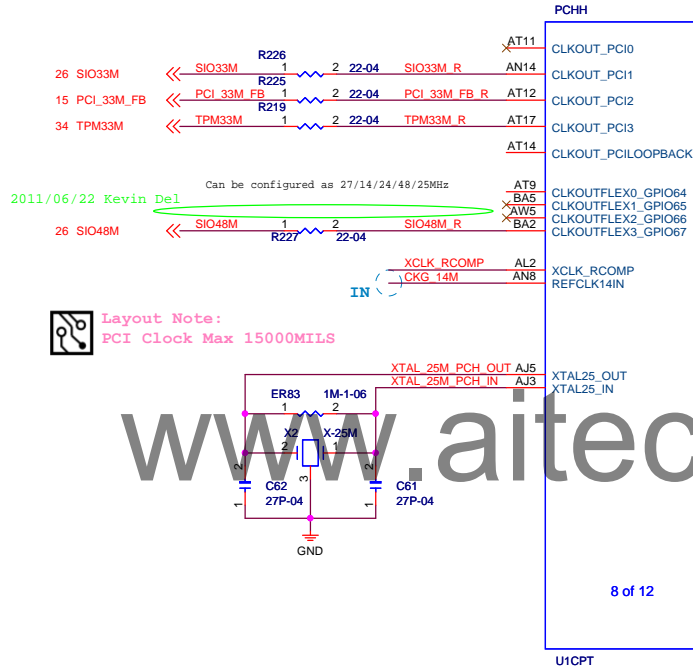
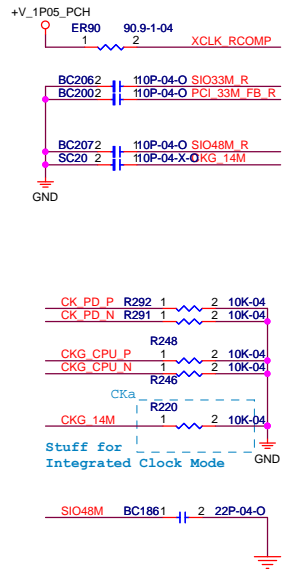


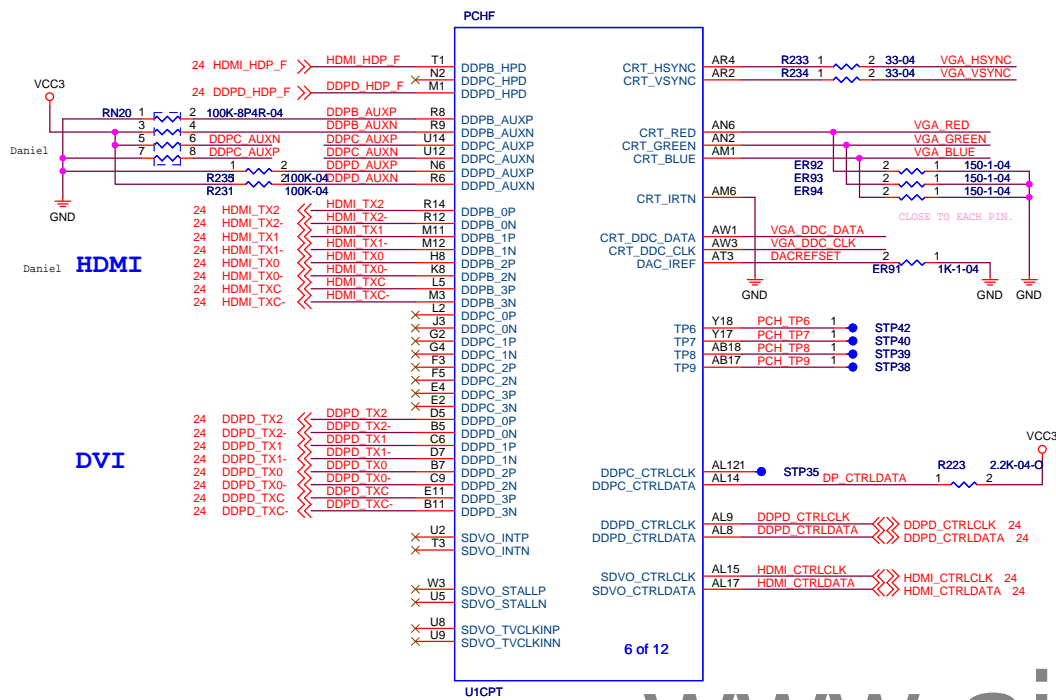
Buffer Through Mode / Integrated Clock Mode have been changed to F/W Strap. Default: Integrated Clock Mode. Doc: Cougar Point Platform Controller Hub (PCH) Family EDS Update V0.7.1



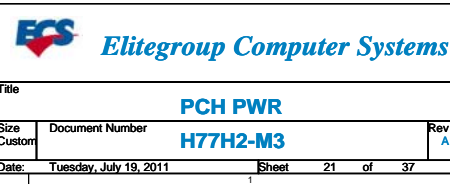
16,26 PWRGD <<> PWRGD FROM SIO
5,32 FP_RST_L <<> SYS_RST_L

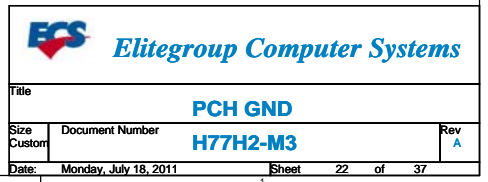






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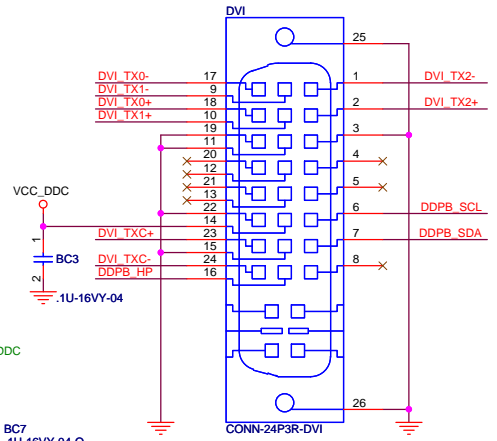
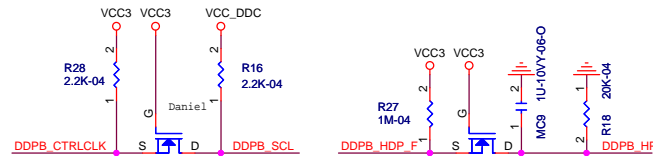
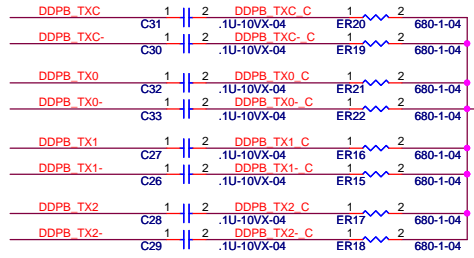




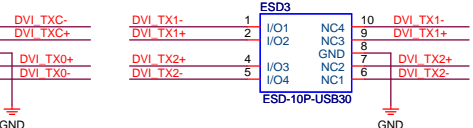
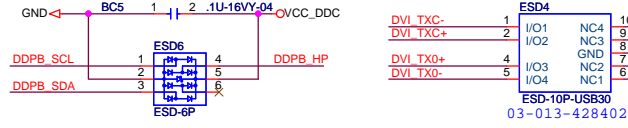
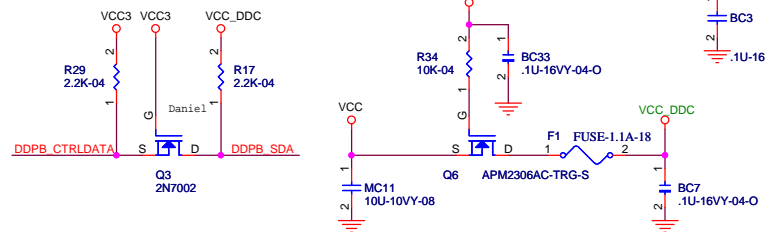
External Connection

20 DDPD_HDP_F << DDPB_HDP_F
20 DDPD_CTRLCLK << DDPB_CTRLCLK
20 DDPD_CTRLDATA << DDPB_CTRLDATA

20 DDPD_TX0 << DDPB_TX0
20 DDPD_TX0- << DDPB_TX0-
20 DDPD_TX1 << DDPB_TX1
20 DDPD_TX1- << DDPB_TX1-
20 DDPD_TX2 << DDPB_TX2
20 DDPD_TX2- << DDPB_TX2-
20 DDPD_TXC << DDPB_TXC
20 DDPD_TXC- << DDPB_TXC-



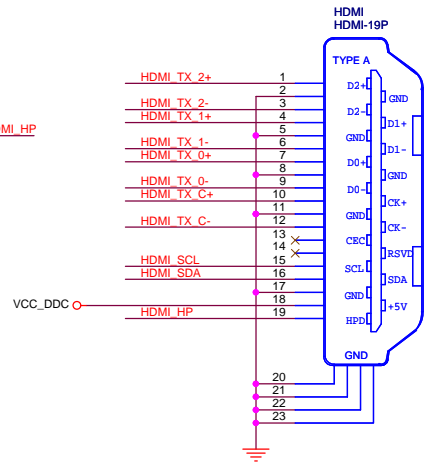
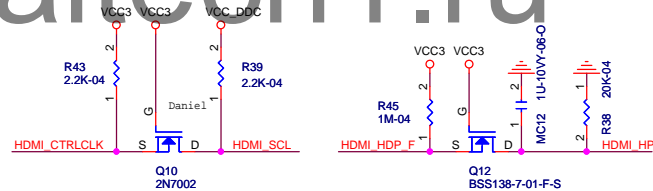
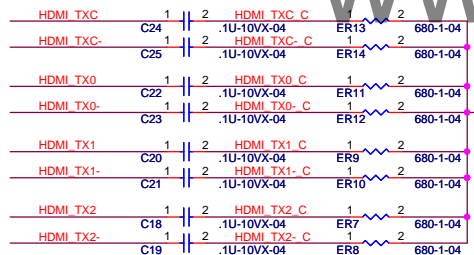
DVI



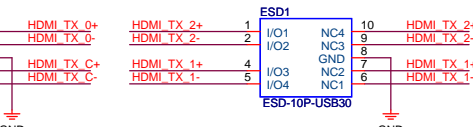
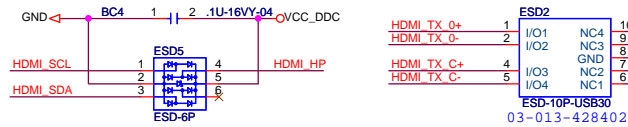
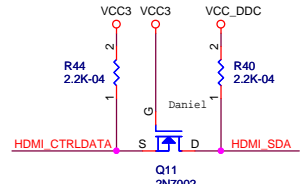
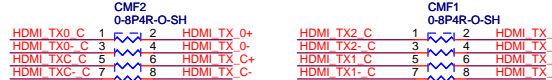
External Connection

20 HDMI_HDP_F << HDMI_HDP_F
20 HDMI_CTRLCLK << HDMI_CTRLCLK
20 HDMI_CTRLDATA << HDMI_CTRLDATA

20 HDMI_TX0 << HDMI_TX0
20 HDMI_TX0- << HDMI_TX0-
20 HDMI_TX1 << HDMI_TX1
20 HDMI_TX1- << HDMI_TX1-
20 HDMI_TX2 << HDMI_TX2
20 HDMI_TX2- << HDMI_TX2-
20 HDMI_TXC << HDMI_TXC
20 HDMI_TXC- << HDMI_TXC-



HDMI



Elitegroup Computer Systems

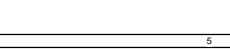
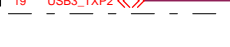
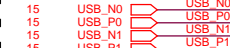
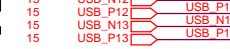
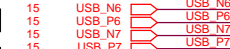
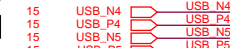
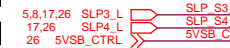
DVI / Rear USB

Document Number: **H77H2-M3**

Date: Monday, July 18, 2011

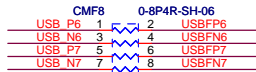
Sheet 24 of 37

External Connection

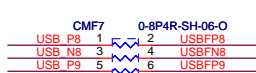


2011/07/11 Kevin Del

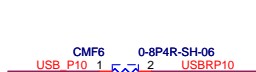
FRONT_SIDE



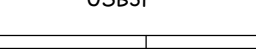
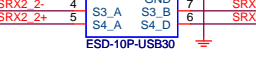
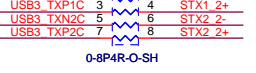
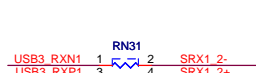
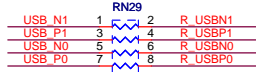
FRONT_SIDE



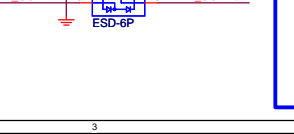
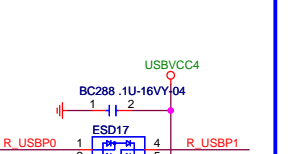
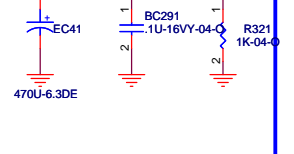
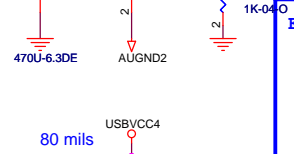
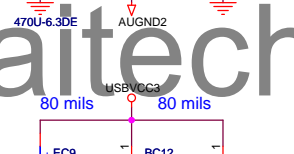
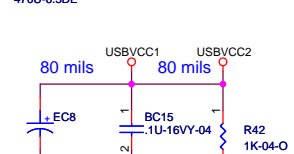
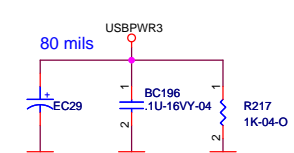
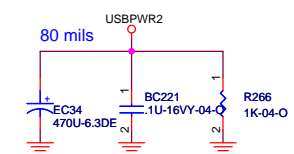
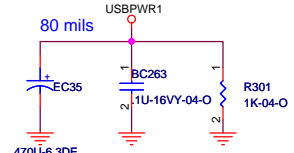
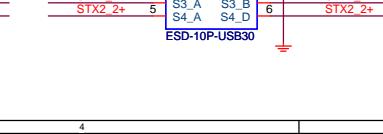
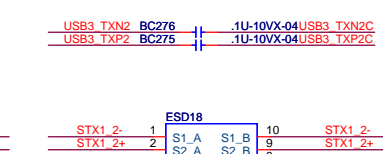
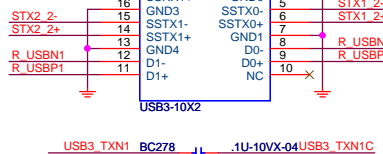
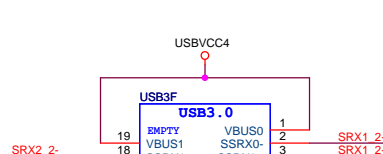
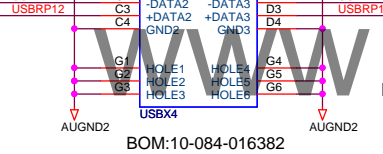
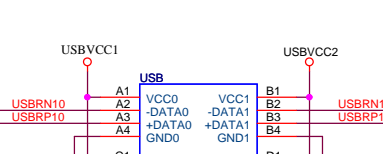
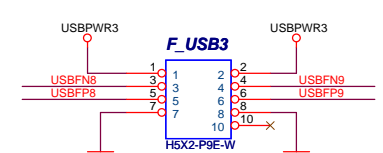
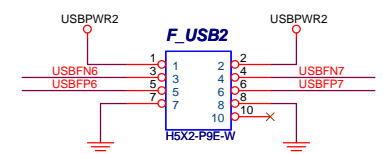
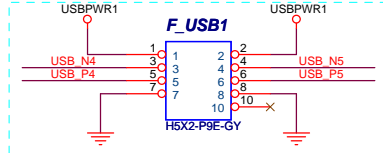
FRONT_SIDE



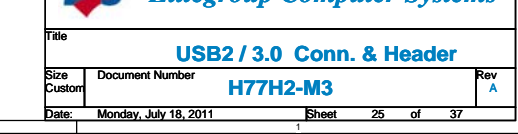
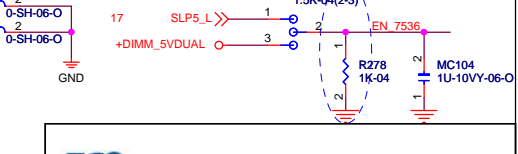
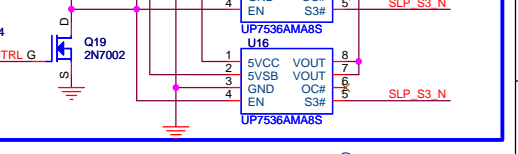
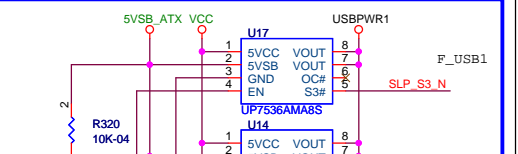
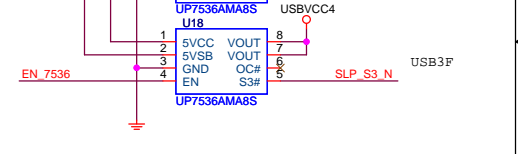
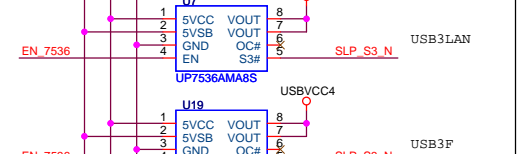
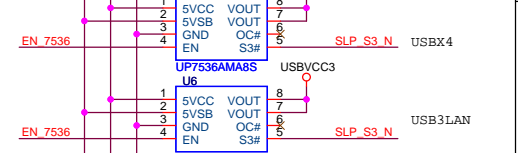
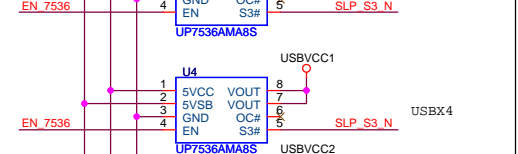
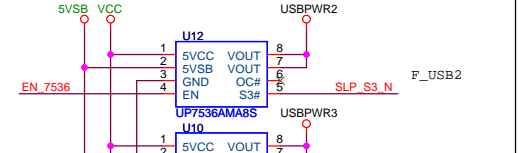
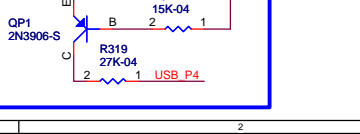
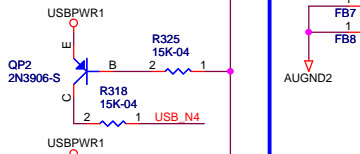
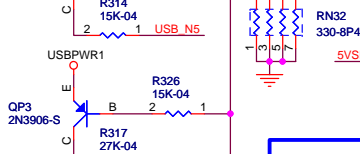
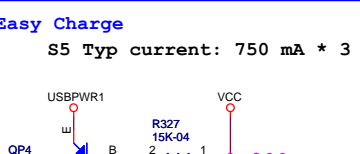
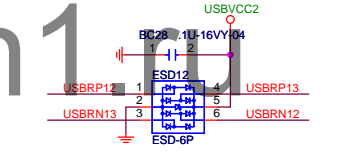
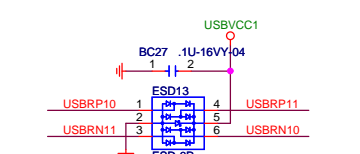
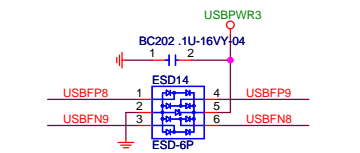
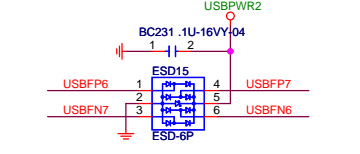
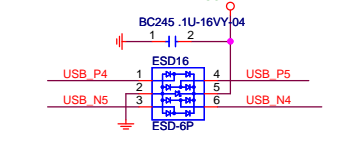
REAR USB 4 Port



Easy Charge



Close to Header or Connector

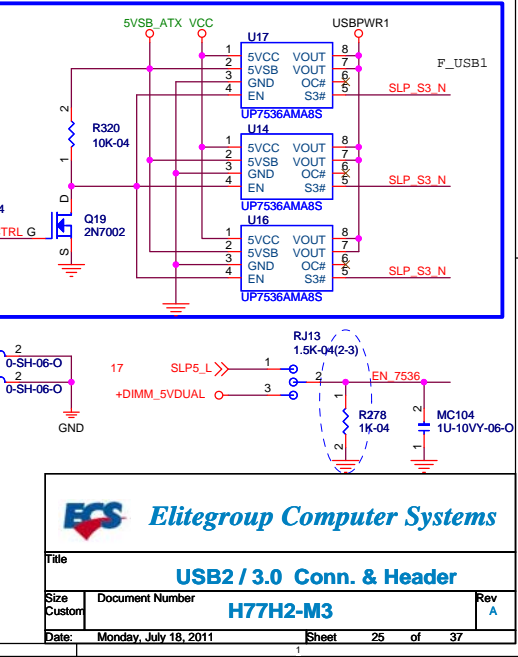
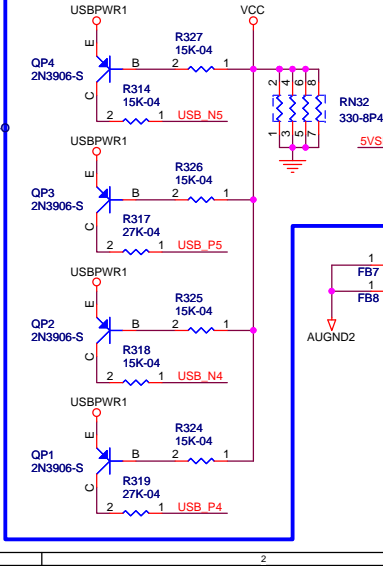


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BOM:10-084-016382

Easy Charge

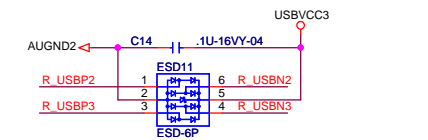
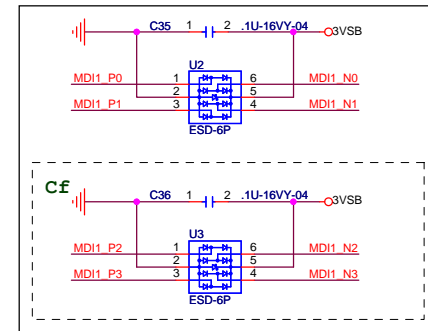
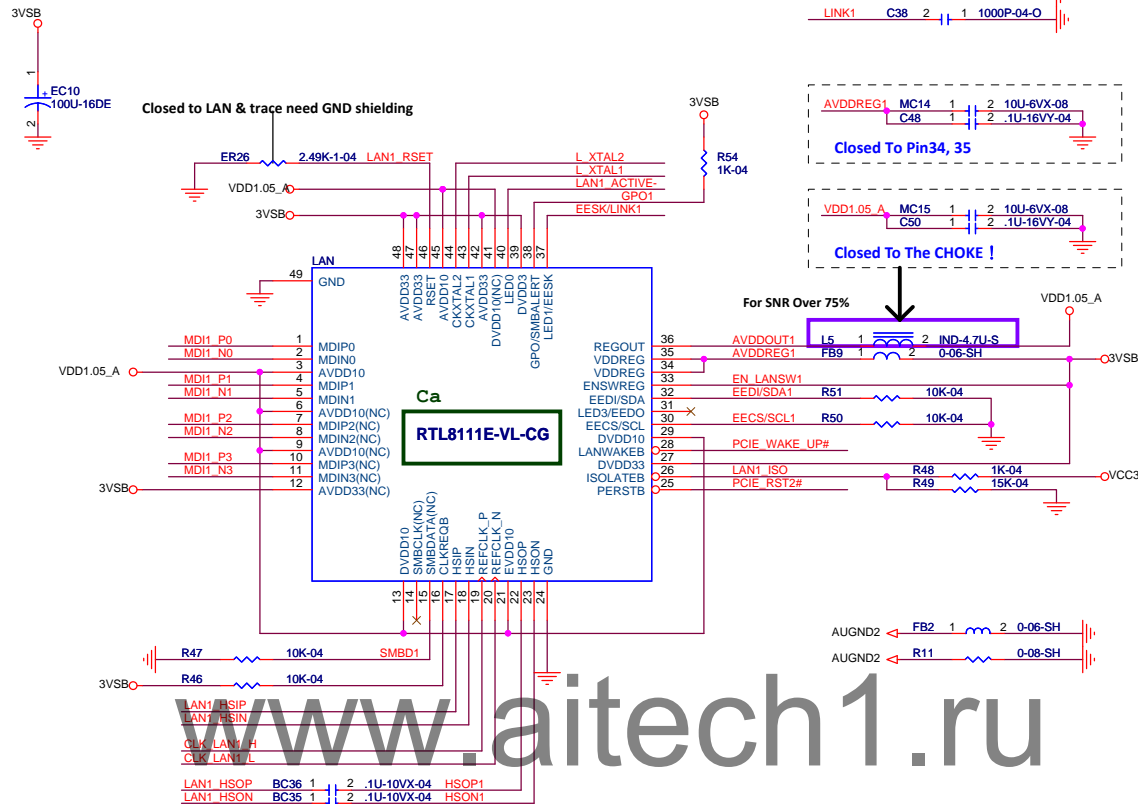
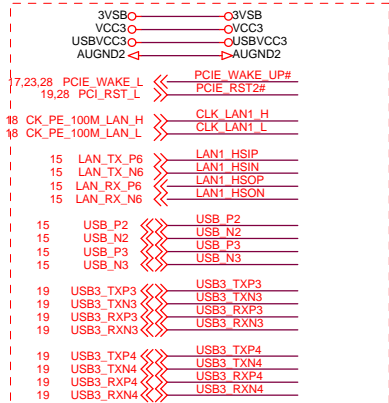
S5 Typ current: 750 mA * 3



Elitegroup Computer Systems

Title	USB2 / 3.0 Conn. & Header	Rev	A
Size	Document Number	H77H2-M3	
Custom			
Date	Monday, July 18, 2011	Sheet	25 of 37

External Connection

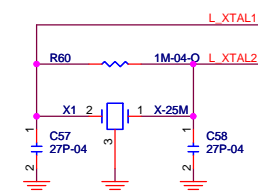


When you found some bug, please inform Ren(ext:26150) to update circuit.
新手提醒:

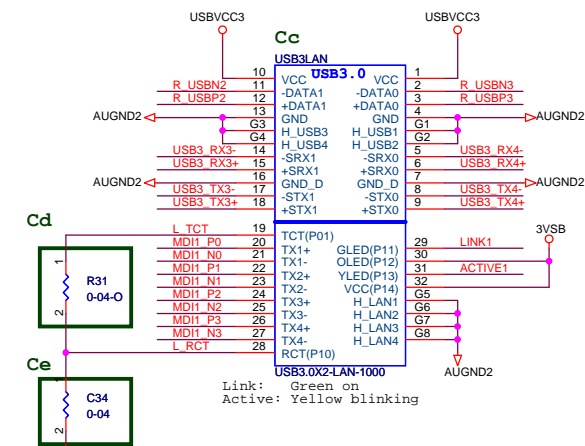
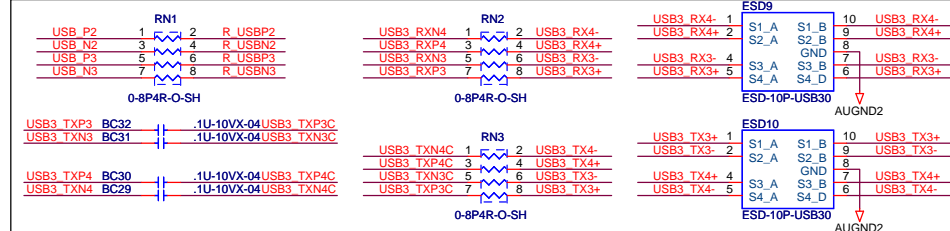
LAN_HSOP/N請接到SB的PCIE RX端

LAN_HSIP/N請接到SB的PCIE TX端

LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap



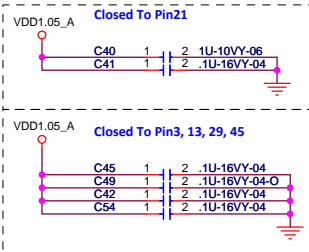
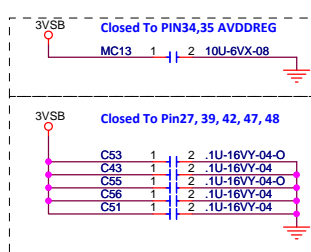
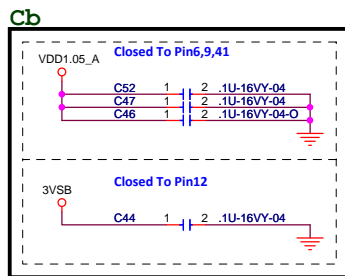
USB3.0



BOM Difference

	RTL8111E-VL 1000M	RTL8105E-VL 10/100M
Ca	RTL8111E-VL-CG	RTL8105E-VL-CG
Cb	V	X
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-25VX-04
Cf	V	X
Cg		

DEFAULT



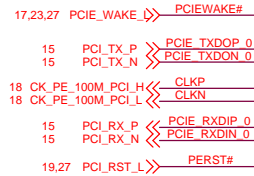
Elitegroup Computer Systems

Title		
PCIE LAN / AR8151-B		
Size	Document Number	Rev
Custom	H77H2-M3	A
Date:	Monday, July 18, 2011	Sheet 27 of 37

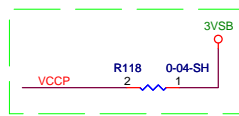
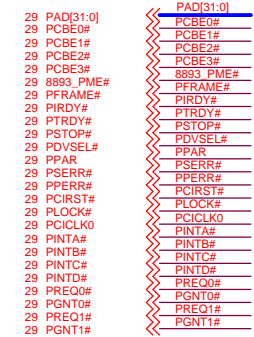
External Connection



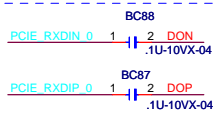
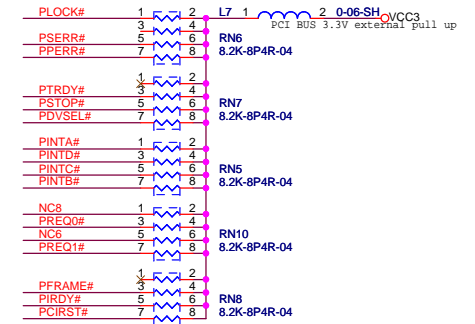
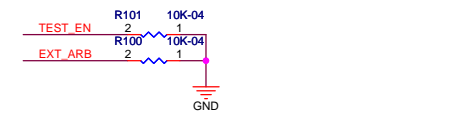
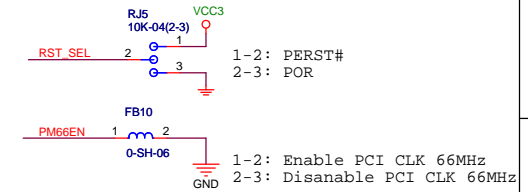
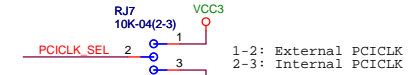
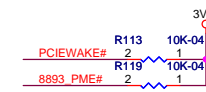
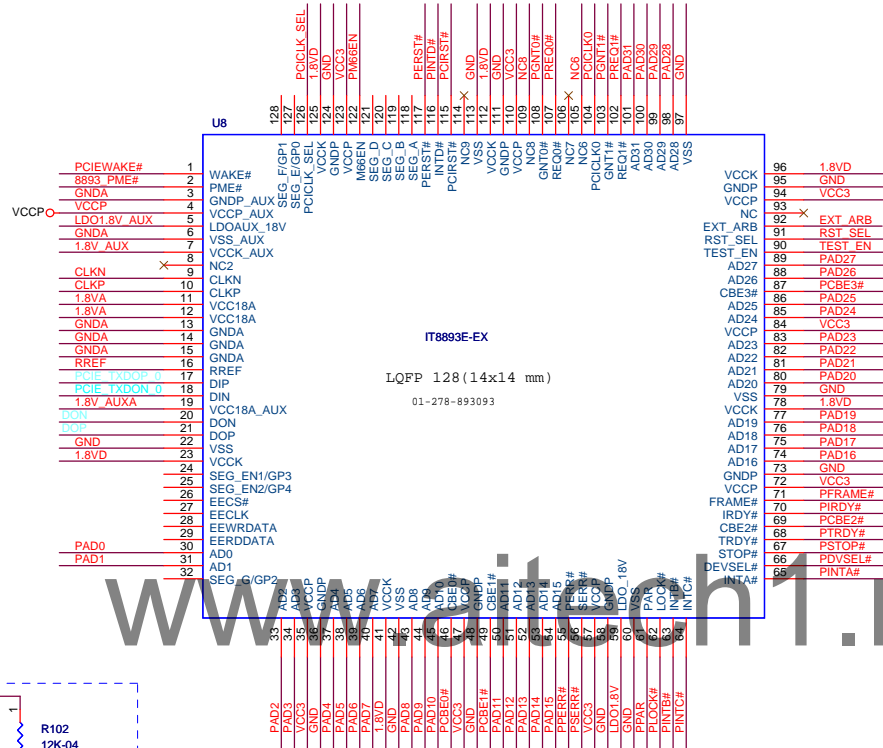
PCIE



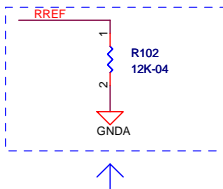
PCI slot



PCB layout note:
Connect to PCIE
PERST# Signal



PCB layout note:
PCIE TX signals
Close to chip



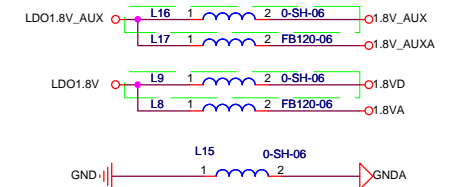
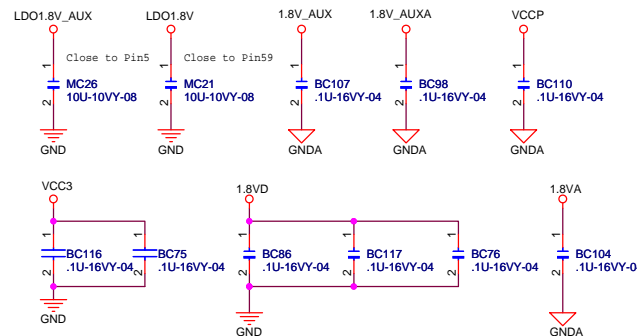
PCB layout note:
Close to chip

PCIE DIP;DIN;DOP;DON PCB layout note:

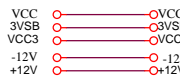
To meet Differential Impedance :85 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
PCIE DIP and DIN trace width:9.5 mils
PCIE DOP and DON trace width:9.5 mils
Space between DIP/DIN and DOP/DON:14.5 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 2 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inches (Max.)

PCIE CLK PCB layout note:

To meet Differential Impedance :100 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
CLKP and CLKN trace width:7 mils
Space between CLKP and CLKN:14 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 4 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inches (Max.)

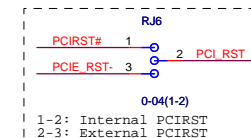
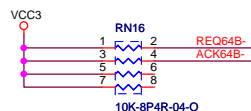
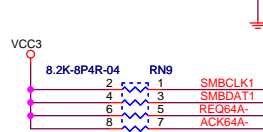
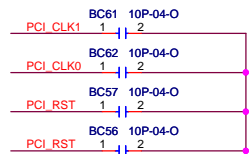
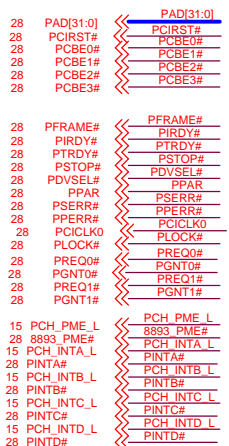


External Connection

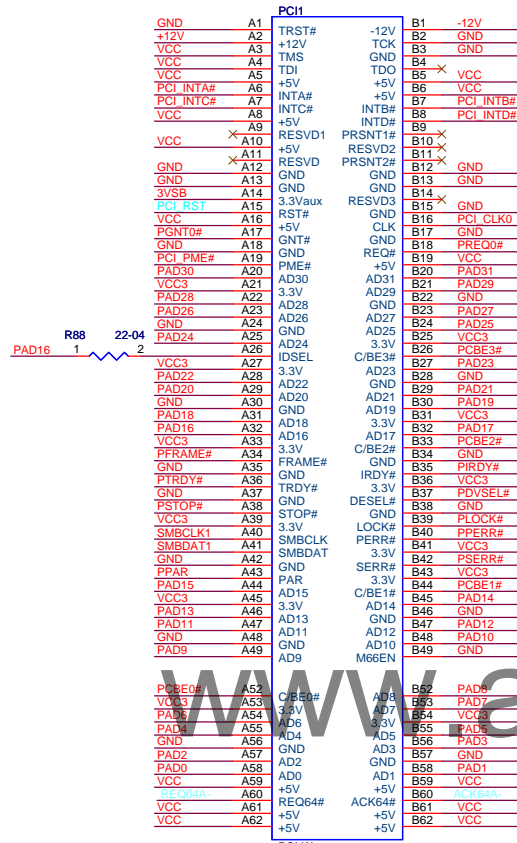


19,23,34 PCIE_RST- PCIE_RST-

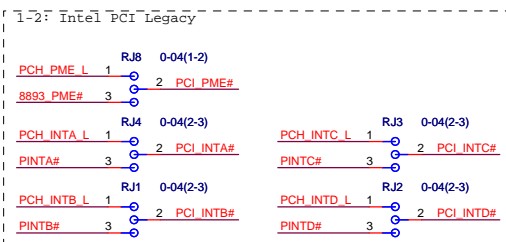
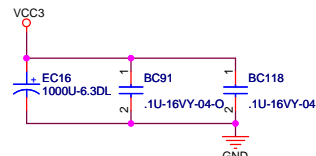
COMMON



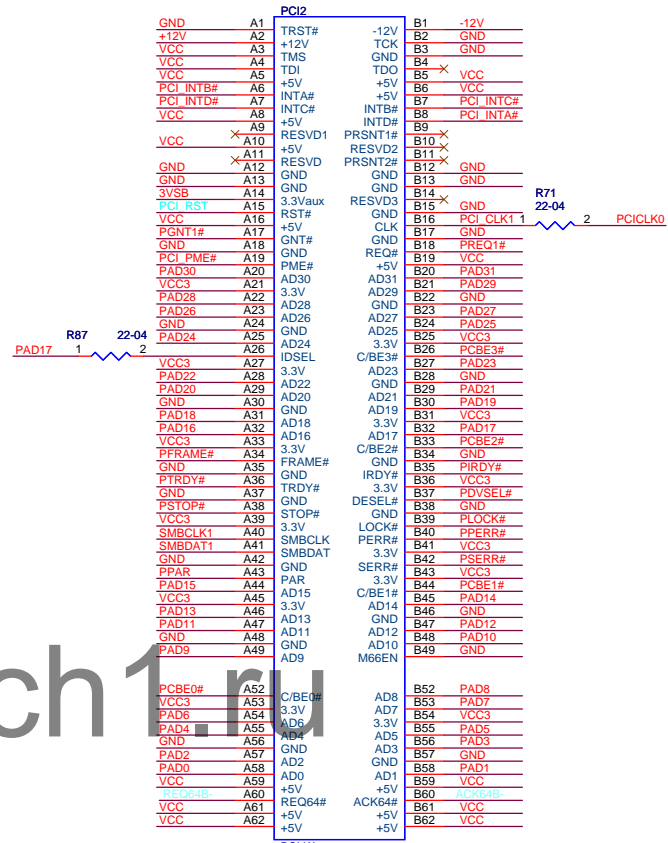
PCI1



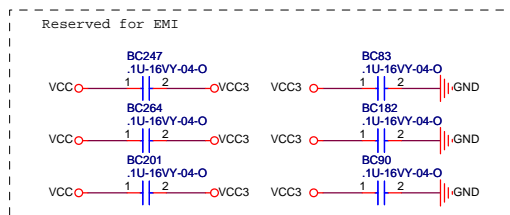
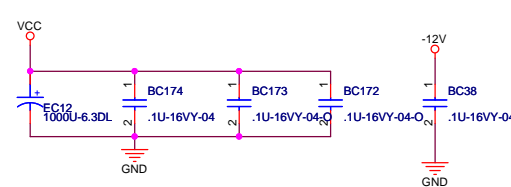
PCI1:REQ0;GNT0 IDSEL:16 INT:ABCD



PCI2

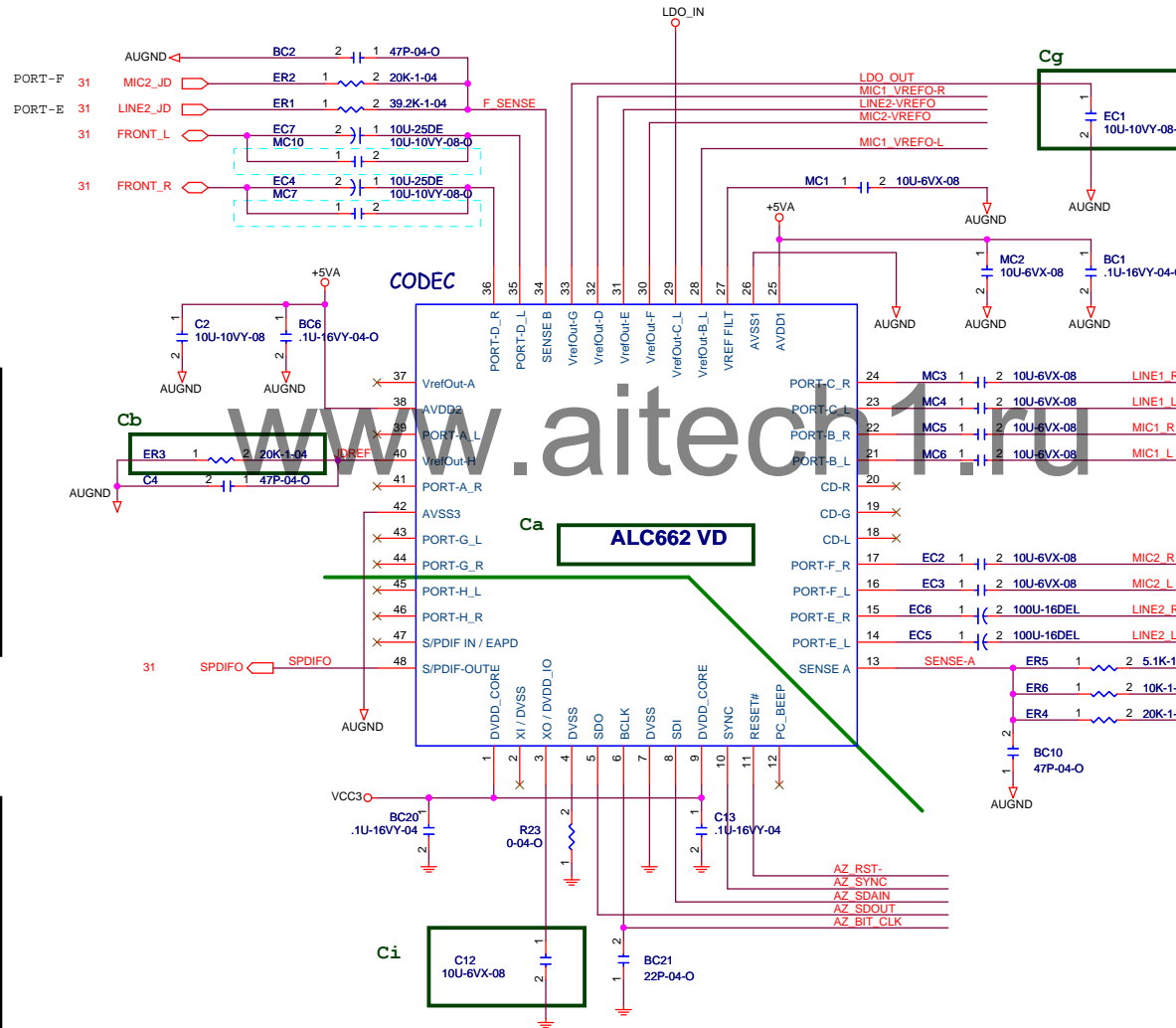
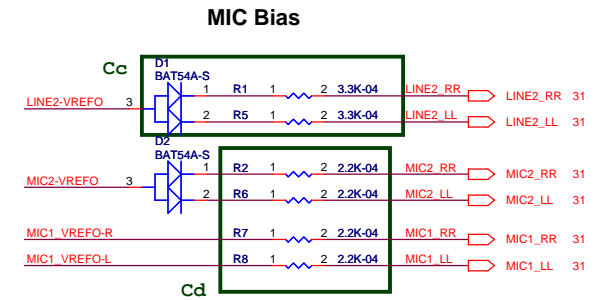
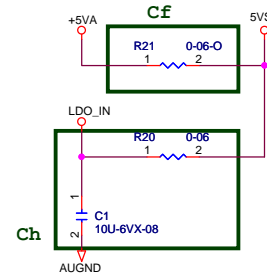
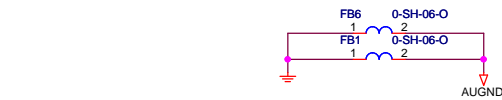
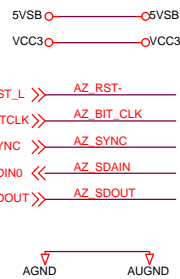


PCI2:REQ1;GNT1 IDSEL:17 INT:BCDA



Title		Slot PCI1 / 2	
Size	Document Number	H77H2-M3	
Custom		Rev A	
Date:	Monday, July 18, 2011	Sheet	29 of 37

External Connection



Pin Difference

Pin	ALC662 VD	VT1705CE
3	REG VREF	GPIOL
4	GPIOL	DVSS
25	LDO OUTPUT	LDO VIN
29	LDO VIN	OPTION CAP
33	LINE1 VREF	LDO OUTPUT
37	FRONT VREF ?	NC
38	LDO OUTPUT	LDO VIN
45	DMIC DATA	NC
46	DMIC CLK	NC

BOM Difference

Location	ALC662 VD	VT1705CE
Ca	ALC662-VD0-GR	VT1705CE
Cb	20K-1-04	5.1K-1-04
Cc	V	X
Cd	2.2K-04	3.3K-04
Ce	75-04	16-04
Cf	X	V
Cg	X	V
Ch	V	X
Ci	V	X

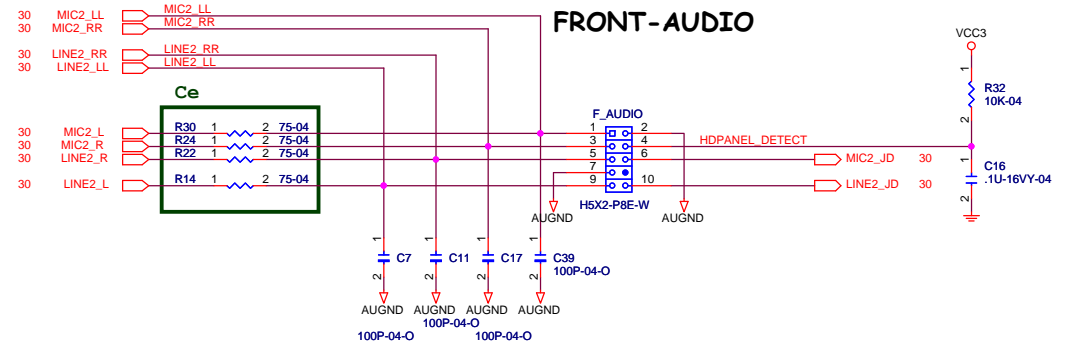
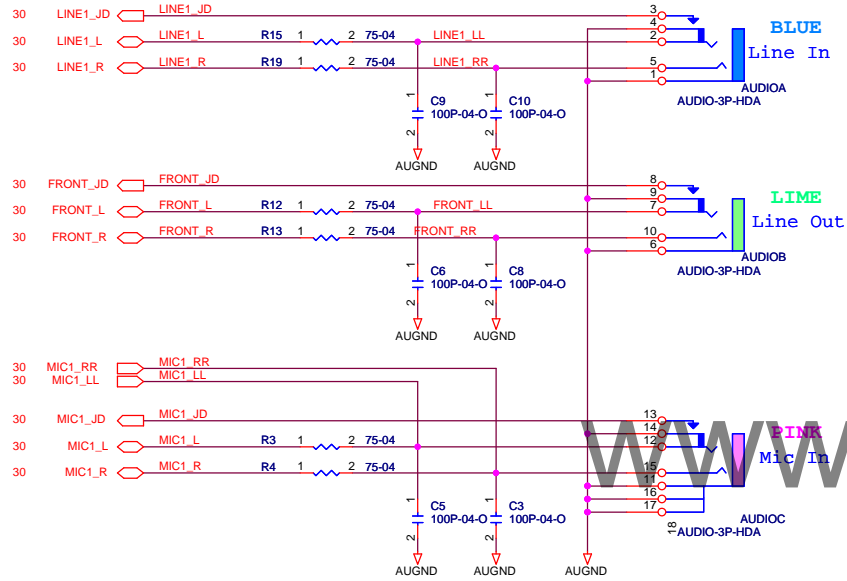
When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

External Connection

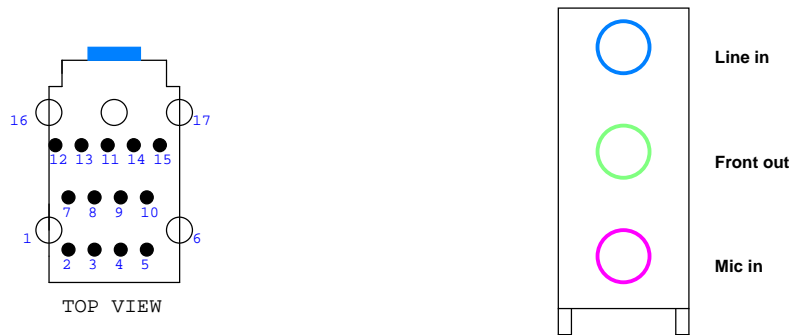
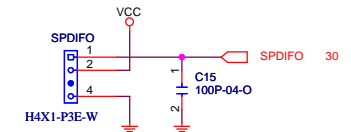
17 FP_AUD_DETECT ← HDPANEL_DETECT

* HDPANEL_DETECT connect to SIO or SB GPIO for AC97 Panel support

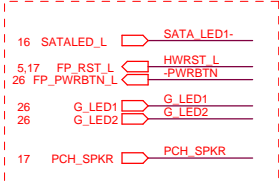
REAR-AUDIO Non re-tasking for rear panel



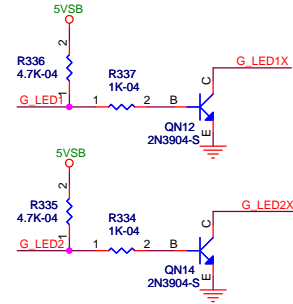
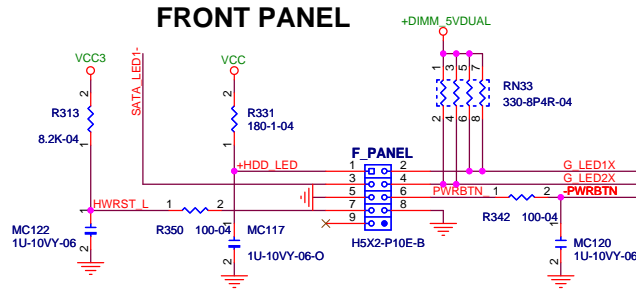
SPDIF-OUT



External Connection

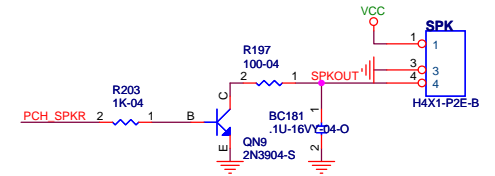


FRONT PANEL



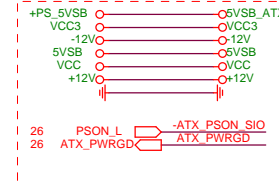
	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
	G	B	YB	OFF	OFF

B: Blinking

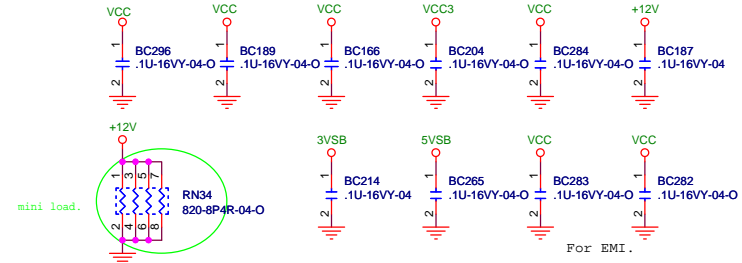
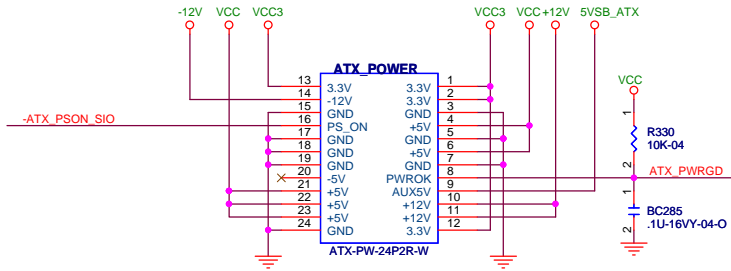


POWER CONNECTOR

External Connection



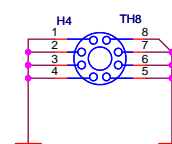
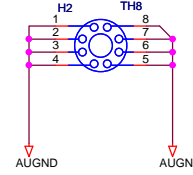
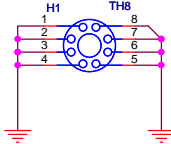
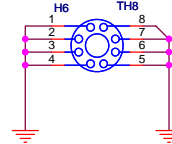
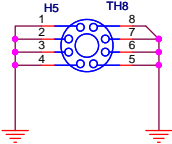
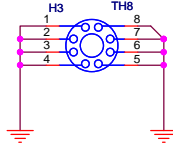
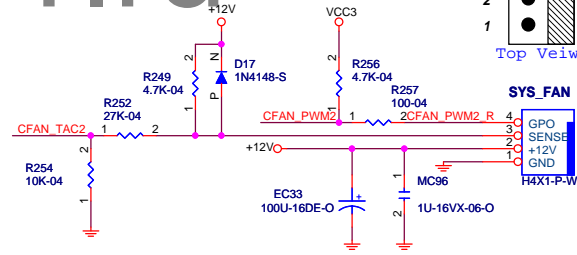
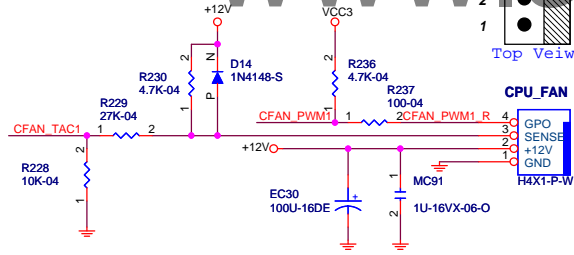
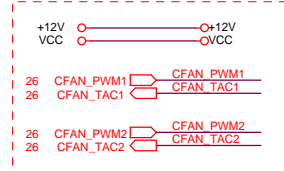
F_PANEL	
1	2
3	4
5	6
7	8
9	X
HDD_LED	RST
	PWR



FAN

Kent 1016

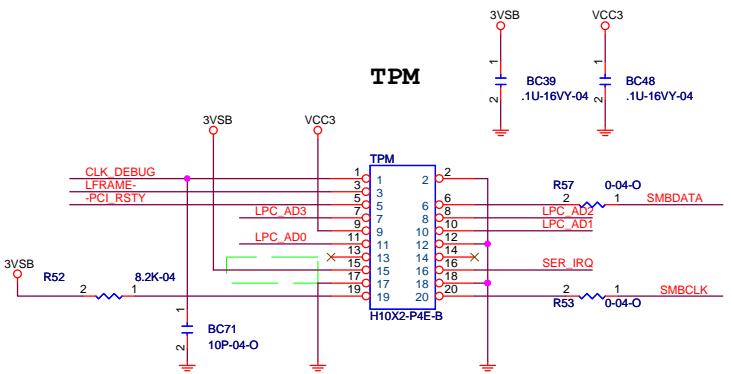
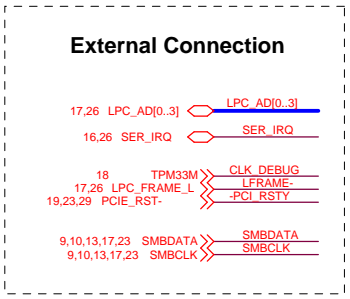
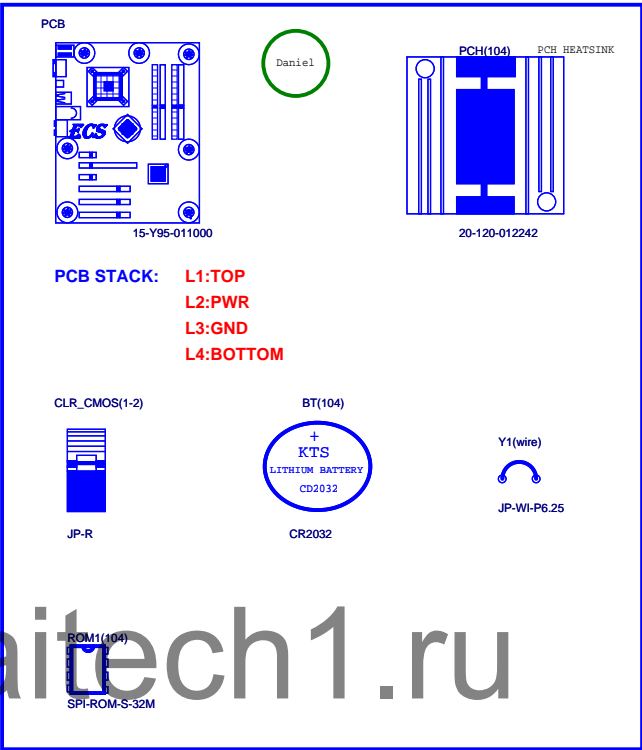
External Connection



Elitegroup Computer Systems

Title		
F_PANEL / FAN / PWR CONN		
Size	Document Number	Rev
Custom	H77H2-M3	A
Date:	Monday, July 18, 2011	Sheet 32 of 37

104 Phase



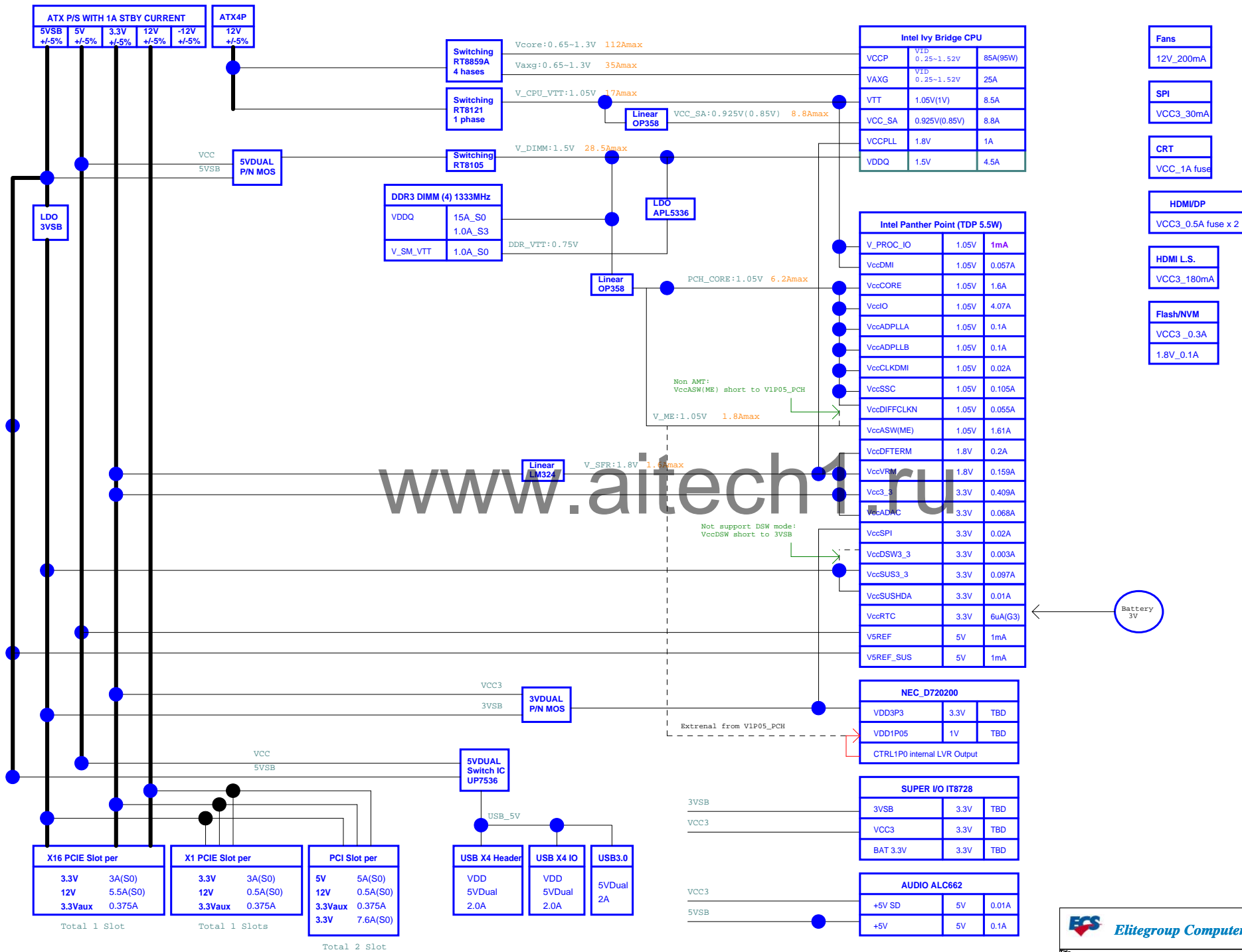
1)Circuit type 1

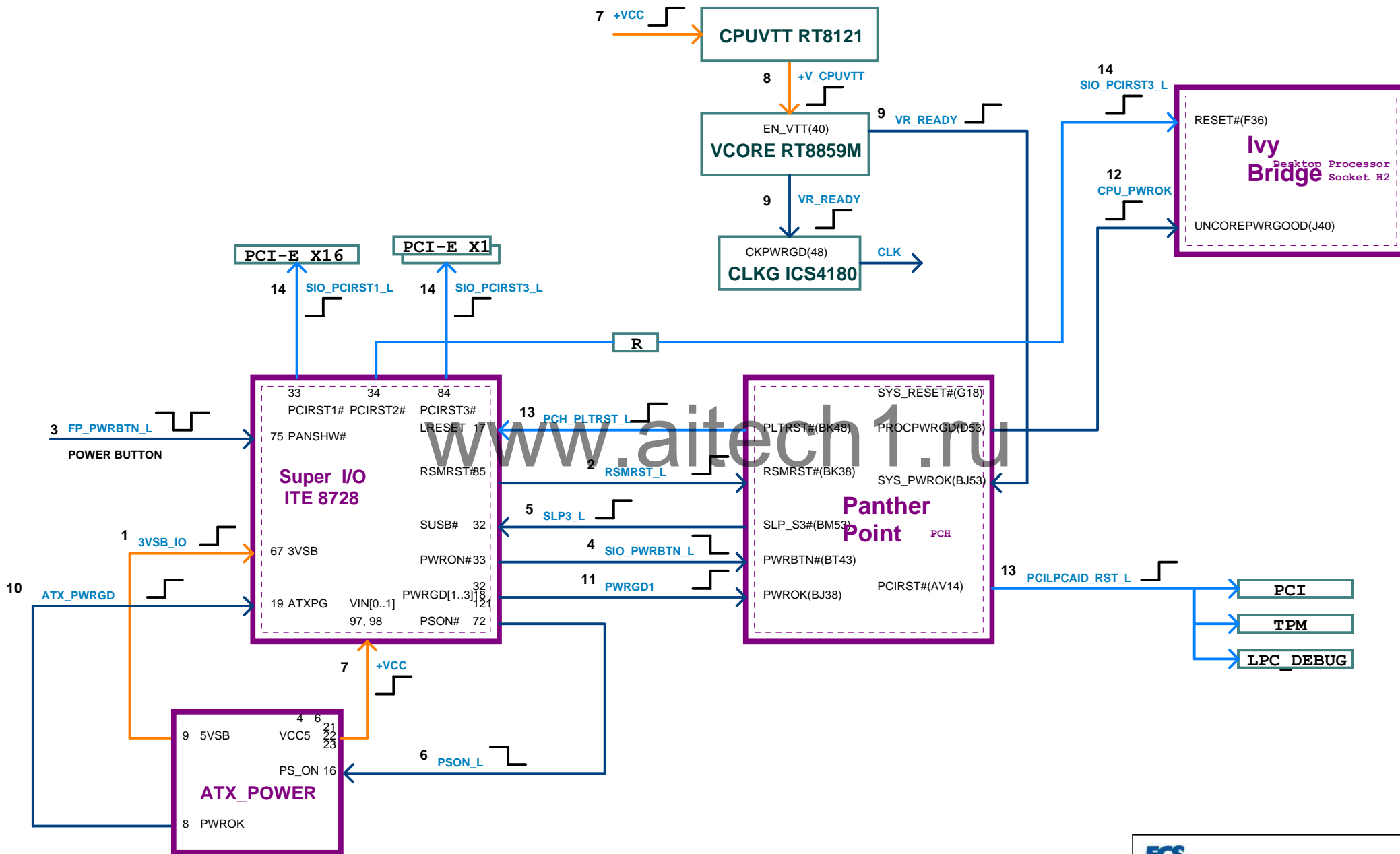
Layer 1:TOP

Layer 2:PWR

Layer 3:GND

Layer 4:BOTTOM





NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

